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Si-SiO2 interface behavior in n-MOSFETs with screening potential during high-field injection

Purushothaman Srinivasan
New Jersey Institute of Technology

ABSTRACT

Si-SiO_2 INTERFACE BEHAVIOR IN n-MOSFETS WITH SCREENING POTENTIAL DURING HIGH-FIELD INJECTION

by

Purushothaman Srinivasan

This work investigates the screening of hot carrier stress degradation in n-channel MOSFETs when the devices were exposed to plasma processing. Devices with various antenna ratios were subjected to current stress (both gate injection and substrate injection) while the source and drain terminals were reverse biased by a screening potential followed by hot carrier stress. It was observed that screening of the drain edge was effective for both gate injection and substrate injection at different screening potentials. The hot carrier lifetime is directly related to interface state density (Dit), measured by charge pumping method. The results suggest that hot electron degradation could be severe or mild for devices affected by plasma damage depending on their exposure to the level of screening potential.

This work also investigates the screening of Si-H bond concentration for polarity-dependent high field electron injection under effective screening potentials. It was observed that Si-H bond concentration varies based on the screening of the source and the drain edges during current stress when a reverse bias potential is applied to the source and drain terminals. The interface state density (D_{it}), measured by charge pumping method, is found to have strong dependence on the concentration of the Si-H bonds. Hot carrier stress that significantly contributes to Si-H bond breaking confirmed the effective screening. The results also indicate that Si-H bond breaking mechanism during screening is dependent on the polarity of the current stress and the screening potential applied.

$Si-SiO_2$ INTERFACE BEHAVIOR IN n-MOSFETS WITH SCREENING POTENTIAL DURING HIGH-FIELD INJECTION

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Purushothaman Srinivasan

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$Si\text{-}SiO_2$ INTERFACE BEHAVIOR IN n-MOSFETS WITH SCREENING POTENTIAL DURING HIGH-FIELD INJECTION

Purushothaman Srinivasan

Dr. Durgamadhab Misra, Thesis Advisor — Date
Professor of Electrical and Computer Engineering, NJIT

Dr. Leonid Tsybeskov, Committee Member — Date
Associate Professor of Electrical and Computer Engineering, NJIT

Dr. Marek Sosnowski, Committee Member — Date
Professor of Electrical and Computer Engineering, NJIT

BIOGRAPHICAL SKETCH

Author: Purushothaman Srinivasan

Degree: Master of Science

Date: January 2004

Undergraduate and Graduate Education:

- Master of Science in Electrical Engineering
  New Jersey Institute of Technology, Newark, NJ, 2004

- Bachelor of Technology in Electronics and Communication
  Pondicherry Engineering College, Pondicherry, India, 1999

Major: Electrical Engineering

P. Srinivasan, B. Vootukuru and D. Misra – "Si-SiO_2 interface behavior in n-MOSFETs with reverse biased voltage during high field and electron injection" – Oct 12-16th, 204th meeting of Electrochemical Society, Orlando, USA.

P. Srinivasan, B. Vootukuru and D. Misra – "Impact of High Field and Hot Electron Injection on Si-H Bonds at the Si-SiO_2 interface in n-MOSFETs" – Dec 16-20, International Workshop on Physics of Semiconductor Devices , Chennai, India 2003.

P. Srinivasan, B. Vootukuru and D. Misra – "Screening of Si-H Bonds during Plasma Processing" – Dec 8-12, International Semiconductor Device Research Symposium, Washington DC,USA, 2003.

P. Srinivasan, B. Vootukuru and D. Misra – "Screening of hot electron effect during plasma processing" – Jan 5-9,VLSI design conference, Mumbai, India 2004.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

The rapid progress in semiconductor integrated circuit technology is attributed to the ability to scale the devices. Scaling of devices has various benefits in terms of device dimensions, impurity concentrations, current density, capacitance, delay time, power dissipation and power-delay product. A key concept in scaling, is that the various structural parameters of the MOSFET should be scaled in concert if the device is to function properly. For example, if the lateral dimensions W and L (channel length and width) are reduced by a factor K, then the vertical dimensions such as the source/drain junction depths and insulator thickness should also reduce by the same factor K. For ideal scaling, power supply voltages should also be reduced to keep the electric field constant which is not possible in practice due to system-related constraints. The longitudinal electric fields in the pinch-off region and the transverse electric fields across the gate oxide, increase with MOSFET scaling. A variety of problems arise which are generically known as hot electron effects and short channel effects.

Plasma processing is widely used in manufacturing of such scaled VLSI devices for etching of polysilicon, oxide and metal films, oxide deposition, sputter pre-clean, photoresist stripping and even ion implantation. During plasma processing, devices fabricated on wafers are directly exposed to plasma. The oxide of the MOSFET degrades due to this processing. So it is important to understand this degradation in order to have better devices.

1.2 Objective of the Work

The objective of this work is to investigate and understand the Si-SiO_2 interface behavior of the MOSFETs under the plasma processing conditions existing at the source and drain antenna terminals. By applying a reverse biased potential which simulate the voltages generated at the source and drain antenna due to plasma charging, with a subsequent high field injection either at the gate or the substrate, the degradation can be studied. The nature of degradation is studied by measuring the interface state density which estimates the trap concentration. The life-time study of these devices helps to understand the reliability of these devices. The effect of this high field injection is also studied by investigating the Si-H bond concentration changes at the interface.

1.3 Organization of the Thesis

This thesis deals with the effect of reverse biased potential at source and drain terminals termed as screening potential at the Si-SiO_2 interface, when the transistors are subjected to DC stress and hot electron stress. It also deals with the Si-H bond concentration variation due to these stresses at the interface.

Chapter 2 deals with the description of a general idea about the need for stresses, the nature and the type of stresses, various injection mechanisms that are available, hot electron effect on the devices.

The third chapter discusses about the experimental steps involved in the measurement of various parameters of the devices at various stages. It also discusses in detail, the measurement setup for the DC current stress and the hot electron stress. Also, it describes the principle underlying the measurement of interface traps through charge

pumping current setup. Interface state density calculations from the charge pumping current are also discussed. Estimation of life time of the devices are also calculated and described in detail.

The next chapter deals with the results obtained by these stresses in detail. The performance of transistors for various antenna ratios is described through the device parameters of the devices. Interface state density results are discussed in detail. The reliability of the devices are then understood by studying the results of the hot carrier life time of these devices.

The chapter on stress induced Si-H bond concentration discusses about the changes in the concentration of Si-H bonds at the interface due to high field injection.

CHAPTER 2

STRESS CONDITIONS IN MOSFETs

2.1 Plasma Processing in Thin Gate Oxides

The degradation of gate oxides in MOS devices due to plasma processing has been observed and attributed to electrical charging. Since the damaged oxide may cause IC yield loss or become more vulnerable to hot-carrier induced degradation, it is important to investigate the relationship of plasma damage and hot carrier effect.

In plasma environment, ions and electrons are collected by metal or polysilicon electrodes which serve as antennas. A steady-state voltage appears on the electrode due to charge collection and resulting electrical stress can destroy the underlying gate oxide by oxide breakdown or weaken it by charge trapping in the oxide as well as due to interface trap generation at the Si-SiO_2 interface. Interface traps and charge trapping can be determined from MOSFET characteristics such as subthreshold swing, threshold voltage or mobility. Quantitative monitoring of the interface traps and charge trapping is important since it involves in the degradation of MOSFET performance and reliability. During plasma processes, the wafer surface collects conduction current from plasma which is composed of ion current and an electron current. Figure 2.1 shows the ion current and electron current as a function of time.

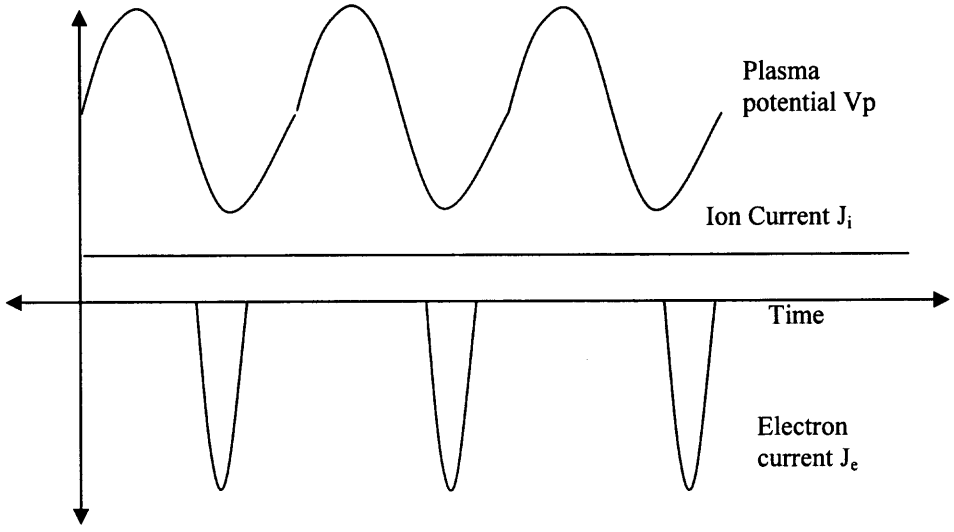


Figure 2.1 Conduction currents during plasma discharge.

The ion current is constant with time and is determined by ion density. Since the plasma potential is higher than the gate potential, the electron current flows only during the short periods when the plasma potential is near its minimum. If the ion and electron currents collected by an electrode balance each other perfectly over the cycle, plasma charging would not be a problem. Charging occurs when the ion and electron currents do not balance each other through the cycle. When the plasma is turned on, the gate voltage increases or decreases over the cycles, depending on which component of the current is larger, until a steady-state oxide voltage is reached when the Fowler-Nordheim (FN) tunneling current through the oxide balances the net current collected by the antenna. This tunneling current degrades the oxide and is always carried by electrons. In general, plasma processing degrades the MOSFET characteristics through Fowler-Nordheim electrical stress of oxide. For positive charging, when the ion current is larger than the average electron current, injection of electrons from the substrate occurs and for negative charging gate electron injection occurs. These electrons generate traps and interface states. In a steady state condition, the gate voltage is a DC with small RF ripples having

amplitudes less than 0.1 V. Therefore plasma charging can be modeled as a DC stress in the oxides.

2.2 DC Stress

High electric field across the oxide leads to trap generation in the bulk of the oxide and at the oxide/substrate interface. The trap generation in oxide and at the interface is a subject of on-going investigations and most high field stress is performed with dc voltage/ current. The interface trap generation depends on various stress conditions applied like stress voltage polarity, stress time, stress type (dc or dynamic). The interface trap generation occurs at a voltage at which the Fowler-Nordheim tunneling of electrons into the oxide starts to build up. This is the direct evidence between the interface trap generation and FN tunneling.

2.2.1 Injection Mechanisms

Six types of injection modes exist for a MOSFET.

1. Channel hot-electron injection (CHE)
2. Drain avalanche hot-carrier (DAHC) injection.
3. Secondary generated hot-electron injection (SGHE).
4. Substrate hot-electron injection (SHE)
5. Fowler-Nordheim (F-N) tunneling injection and
6. Direct tunneling (DT) injection.

CHE injection is due to escape of "lucky" electrons from the channel, causing a significant degradation of the oxide and the Si-SiO_2 interface, especially at low

temperature. DAHC injection results in both electron and hole gate currents due to impact ionization caused by hot holes and hot electrons, giving rise to more severe degradation in room temperature. SGHE injection is due to minority carriers from secondary impact ionization. In F-N injection, the electrons "hop" along in the oxide while going from the Si conduction band to the conduction band of SiO_2, generating F-N current. In DT injection, the electrons in the conduction band of Si tunnels through gate oxide and emerge in the gate, without having to go through the conduction band of the gate oxide.

2.2.2 Fowler-Nordheim Injection

The Fowler-Nordheim tunneling is through a triangular barrier and involves solving Schrödinger equation for the electron wave function. The Fowler-Nordheim tunneling current I_{FN} can be expressed as a function of the electric field in the gate oxide.

$$I_{FN} \alpha E_{ox}^{2} e^{(-B/E_{ox})}$$

Where B is a constant which depends on effective mass and the barrier height. The energy band diagram of Fowler-Nordheim tunneling is shown in Fig. 2.2.

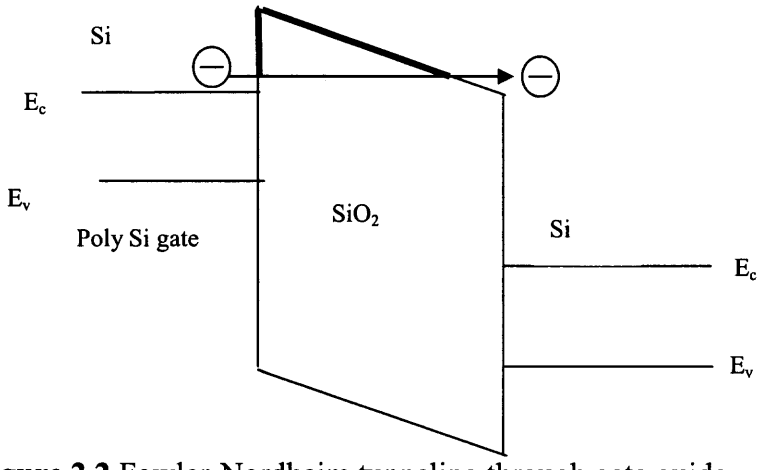


Figure 2.2 Fowler-Nordheim tunneling through gate oxide.

Also the plot of Fowler-Nordheim tunneling leakage current as a function of electric field across the oxide is given in Fig 2.3

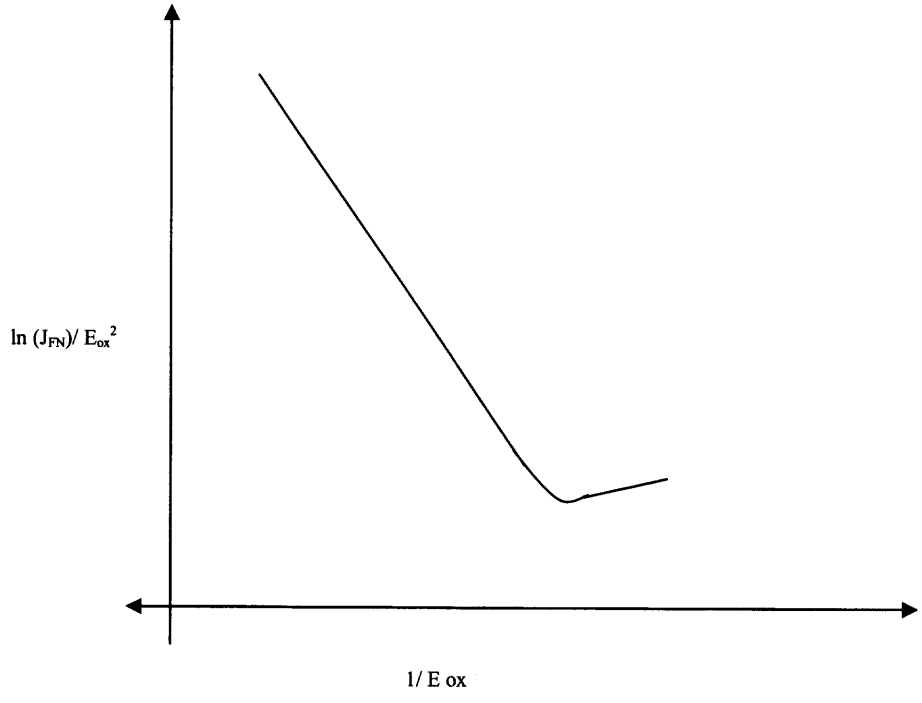


Figure 2.3 Fowler-Nordheim tunneling current.

2.2.3 Gate Injection and Substrate Injection

Based on the injection of electrons, it is classified into two categories as gate injection and substrate injection. If the injection of electrons is from gate to substrate, it is gate injection and if the injection is from substrate to gate then it is called as substrate injection. Figure 2.4 explains these injection mechanisms in the form of energy band diagram.

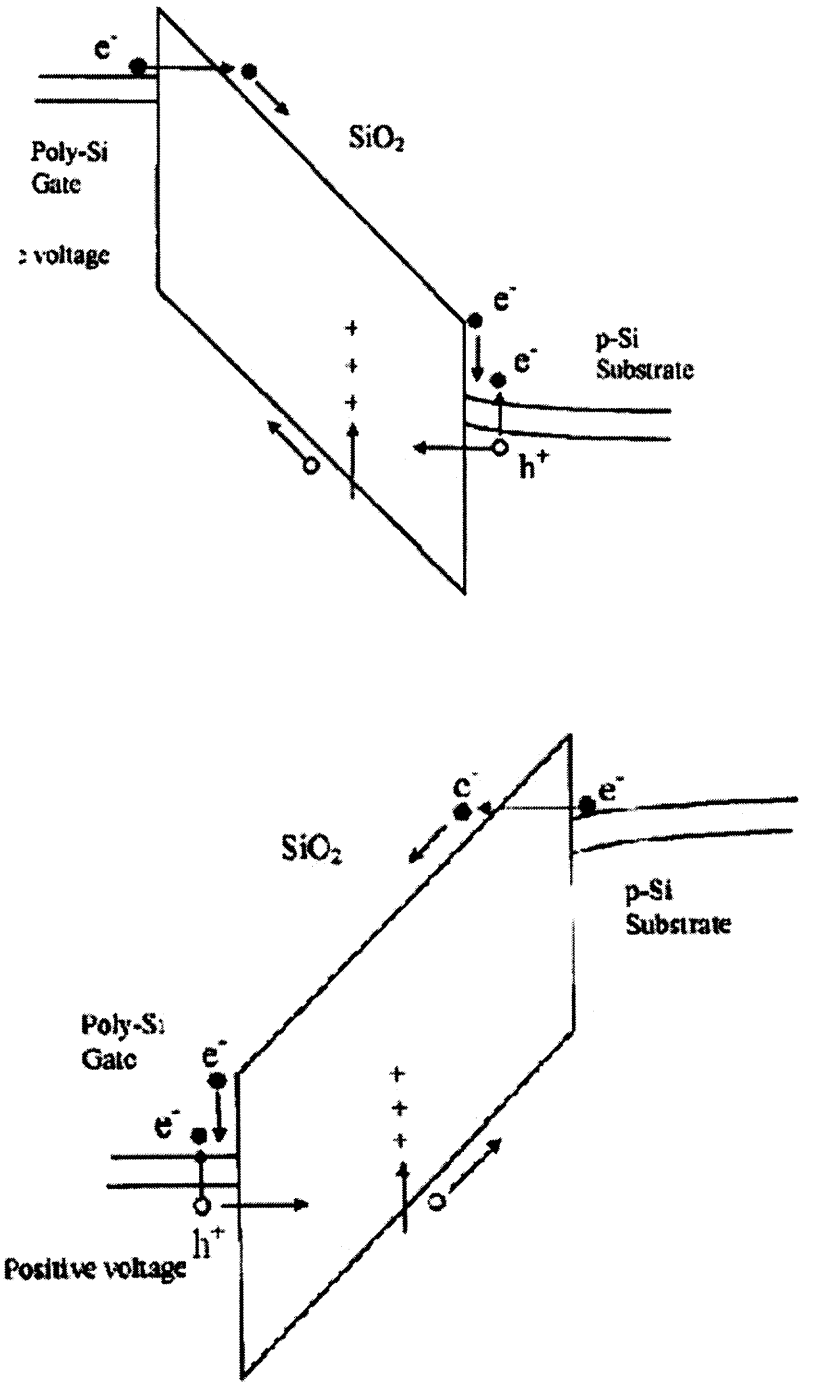


Figure 2.4 Gate injection and substrate injection.

2.3 Hot Electron Effect

When an electron travels from the source to the drain along the channel, it gains kinetic energy at the expense of electrostatic potential energy in the pinch-off region, and becomes a "hot" electron. At the conduction band edge, the electron only has potential energy and as it gains more kinetic energy it moves higher up in the conduction band.

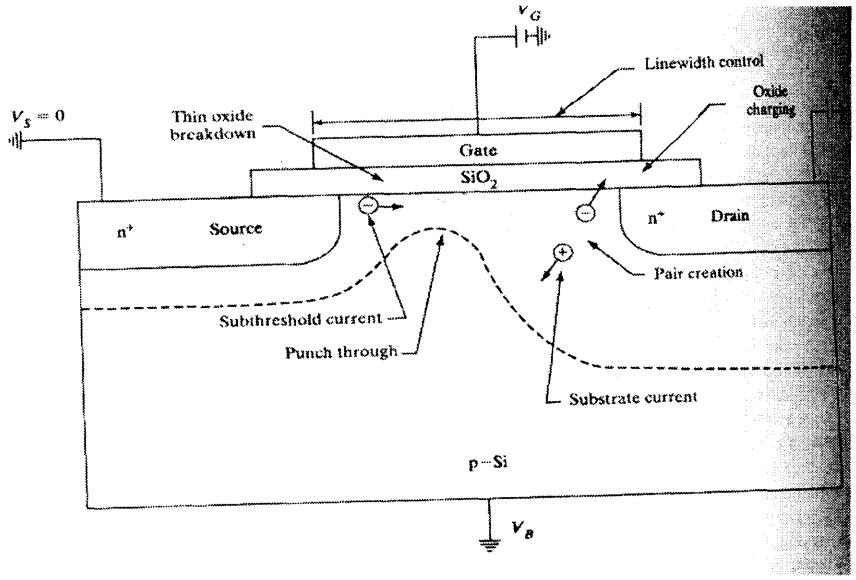


Figure 2.5 Hot electron effect in MOS transistors.

A few of the electrons can become energetic enough to surmount the 3.1 eV potential barrier between the Si channel and gate oxide. Some of these injected hot electrons can go through the gate oxide and be collected as gate current as in Figure 2.5, thereby reducing the input impedance. Some of these electrons can be trapped in the gate oxide as fixed oxide charges. This increases the flatband voltage and therefore the threshold voltage. These energetic hot carriers can break Si-H bonds that exist at the Si-SiO_2 interface, creating fast interface states that degrade MOSFET parameters such as

transconductance and the subthreshold slope, with stress. The result of hot carrier degradation is the increase of threshold voltage and decrease of transconductance. One of the solutions to this problem is to modify the device structure of what is known as Lightly Doped Drain (LDD). By reducing the doping concentration in the source/drain, the depletion width at the reverse-biased drain-channel junction is decreased and the electric field is reduced.

Hot carrier effects are less pronounced in p-channel MOSFETs than for electrons in n-channel devices due to lower channel mobility of holes and hence reduced number of hot holes for the same applied electric field. The lower hole mobility is also responsible for lower drive currents in p-channel rather than n-channel.

One "signature" for hot electron effects is substrate current. As the electron travels towards the drain and become hot, they can create secondary-hole pairs by impact ionization. The secondary electrons are collected at the drain and cause the drain current in the saturation to increase with drain bias at high voltages leading to a decrease of the output impedance. The secondary holes are collected at the substrate as substrate current. This current can create circuit problems such as noise or latch-up in CMOS circuits. As shown, in the Figure 2.6, the substrate current initially increases with gate bias, goes through a peak and then decreases. The reason for this behavior is that, initially, as the gate bias increases, the drain current increases and thereby provides more primary carriers into the pinch-off region for impact ionization. For even higher gate bias, the MOSFET goes from saturation region into the linear region when the fixed V_d drops below the saturation drain voltage. The longitudinal electric field in the pinch-off region drops, thereby reducing the impact ionization rates. Hot electron reliability studies are

always done under "worst case" conditions of peak substrate current.

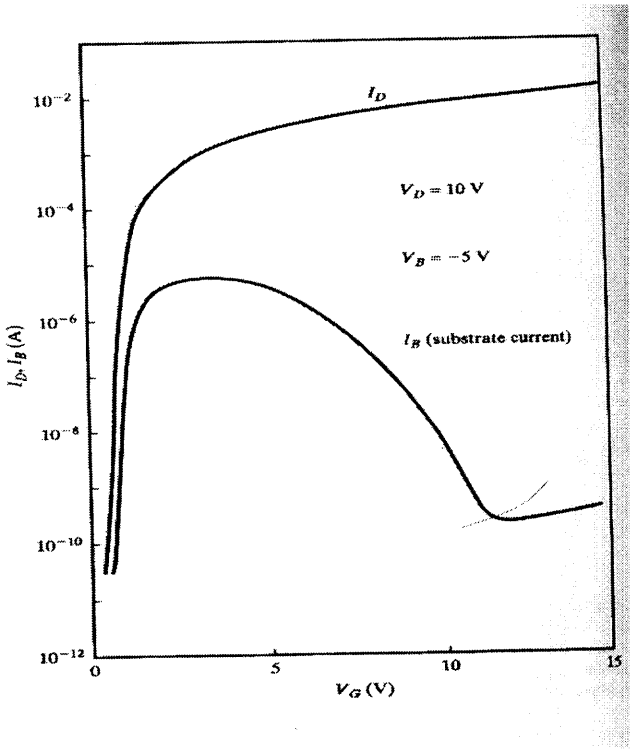


Figure 2.6 Substrate current in a MOSFET.

Hot carrier degradation results from injection of carriers into the gate oxide, which results in a localized and non-uniform buildup of interface states and oxide charges near the drain junction of the transistor. The generated defects produce threshold voltage shift, transconductance degradation, drain current reduction etc. and eventually lead to device failure. Hot carrier degradation is a strong function of internal electric field distributions of the MOSFET. While the lateral electric field near the drain junction is responsible for carrier heating and avalanche, the transverse electric field influence carrier injection into the gate oxide. The reduction of channel length and oxide thickness of the transistor affects the internal electric field distributions and hence the carrier

injection processes. The damage creation and the resulting device degradation thus become a strong function of device dimensions and hence necessary attention is required. Several attempts have been made to understand the effects of MOSFET scaling on Hot Carrier Degradation. The reduction of MOSFET channel length worsens the degradation process. With the reduction in oxide thickness, lesser degradation in terms of charge trapping occurs but carrier heating and avalanche was reported at lower oxide thicknesses.

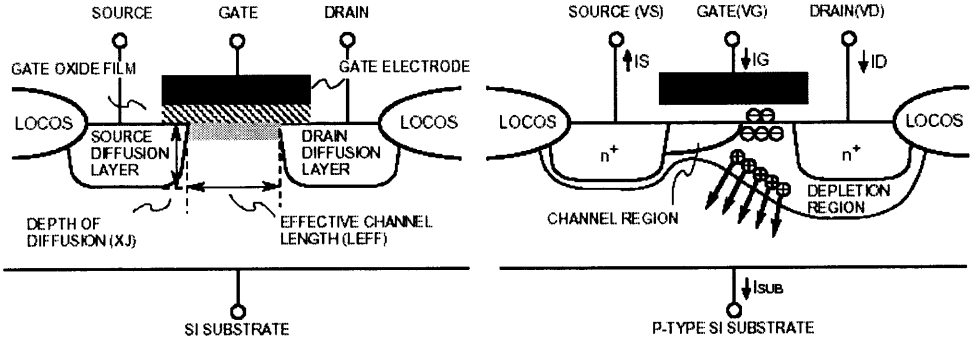


Figure 2.7 Hot electron degradation in MOSFETs.

2.3 Charges at the Si-SiO_2 Interface

There are four general types of charges associated with Si-SiO_2 system shown in the Figure 2.8. They are fixed oxide charges, mobile oxide charges, oxide trapped charges and interface trapped charges.

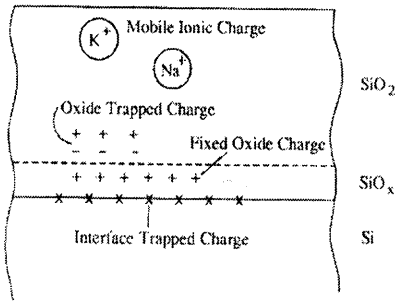


Figure 2.8 Charges at the interface.

2.3.1 Fixed oxide charges

These are positive charges, primarily created due to structural defects in the oxide layer. They are immobile under an applied electric field and does not exchange charge with the silicon when gate bias is varied. This charge ordinarily is dispersed randomly across the interface. The origin is related to the oxidation process and cannot be determined unambiguously in the presence of moderate densities of interface trapped charge. They exist very near to the Si-SiO_2 interface though not exactly at the interface.

2.3.2. Oxide trapped charges

These charges may be either positive or negative due to holes or electrons trapped in the bulk of the oxide. Trapping may result from ionizing radiation, avalanche injection or other similar processes. Unlike fixed charge, oxide trapped charge is generally annealed by low temperature treatments, although neutral traps remain.

2.3.3. Interface trapped charges

They may be either positive or negative charges induced due to structural, oxidation-induced defects, metal impurities or other defects caused by radiation or similar bond breaking processes such as hot electron degradation. The interface trapped charge is located at the Si-SiO_2 interface. Unlike other charges mentioned above, it is in electrical communication with the underlying silicon and can thus be charged or discharged depending on the surface potential. The interface traps change occupancy with gate bias changes and have energy levels distributed throughout the band gap.

2.3.4 Mobile ionic charges

These charges are primarily due to ionic impurities such as sodium, potassium, lithium and possibly hydrogen. Negative ions and heavy metals may contribute to this charge even though they are not mobile below 500 C.

2.4 Si-H Bonds at the Interface

MOSFET degradation is dominated by the generation of acceptor-type interface traps which are localized in a narrow band near the drain and reduce local mobile carrier density. The interface traps responsible for device degradation are generated by hot electrons having energies larger than 3.7 eV. A possible mechanism is that a hot electron breaks a Silicon-Hydrogen bond. If the resultant trivalent silicon atoms recombine with hydrogen, no interface trap is generated. The concentration of Si-H bonds at the interface is in the order of 10^{12} /cm^2.

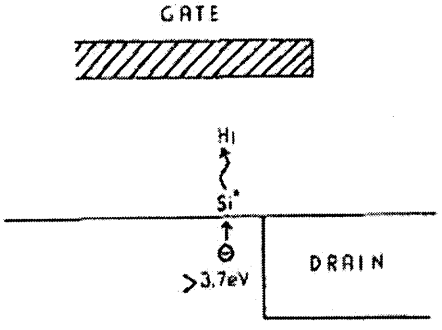


Figure 2.9 Si-H bond breaking at the interface.

More significant types of behavior are being associated with hydrogen at or near the Si-SiO_2 interface.

1. Hydrogen can cross the interface without reaction and passivate dopant atoms in

the Si.

2. If the interface is annealed using FGA (forming gas anneal), introduction of H can passivate defects at the interface via the reaction

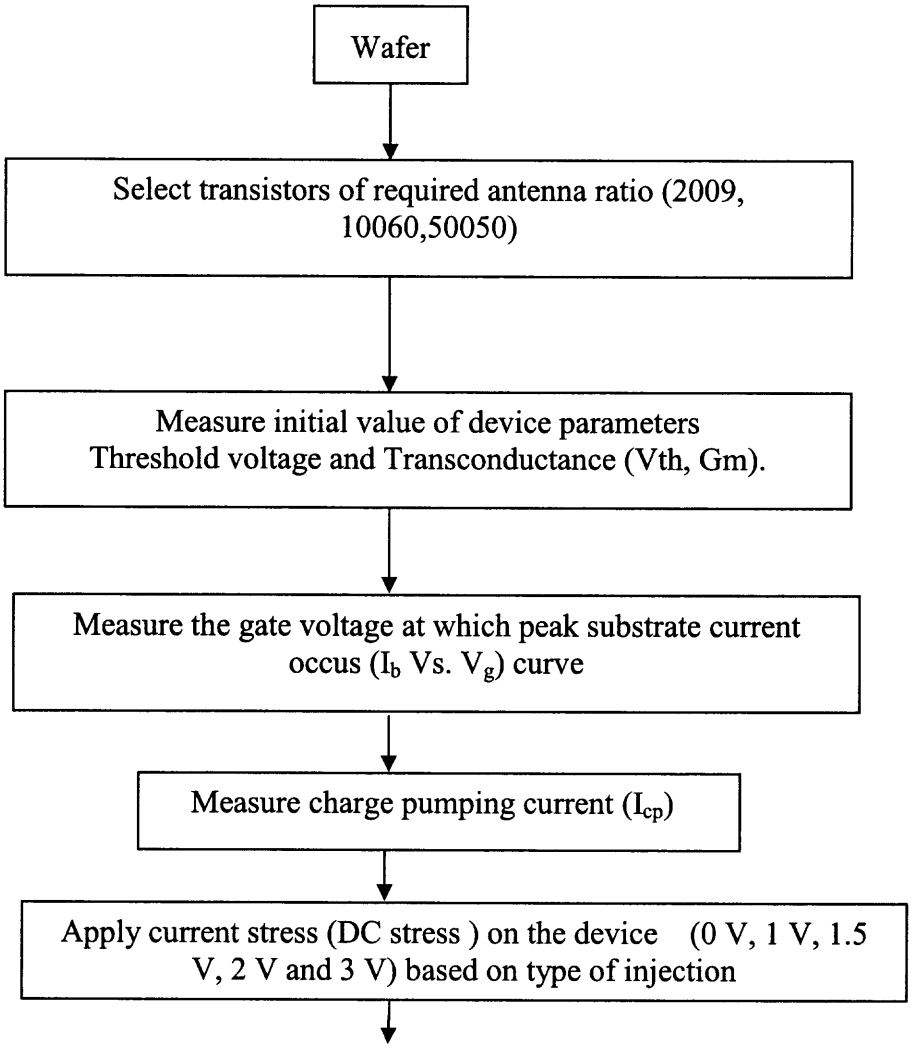
$$D + H \Rightarrow SiH$$

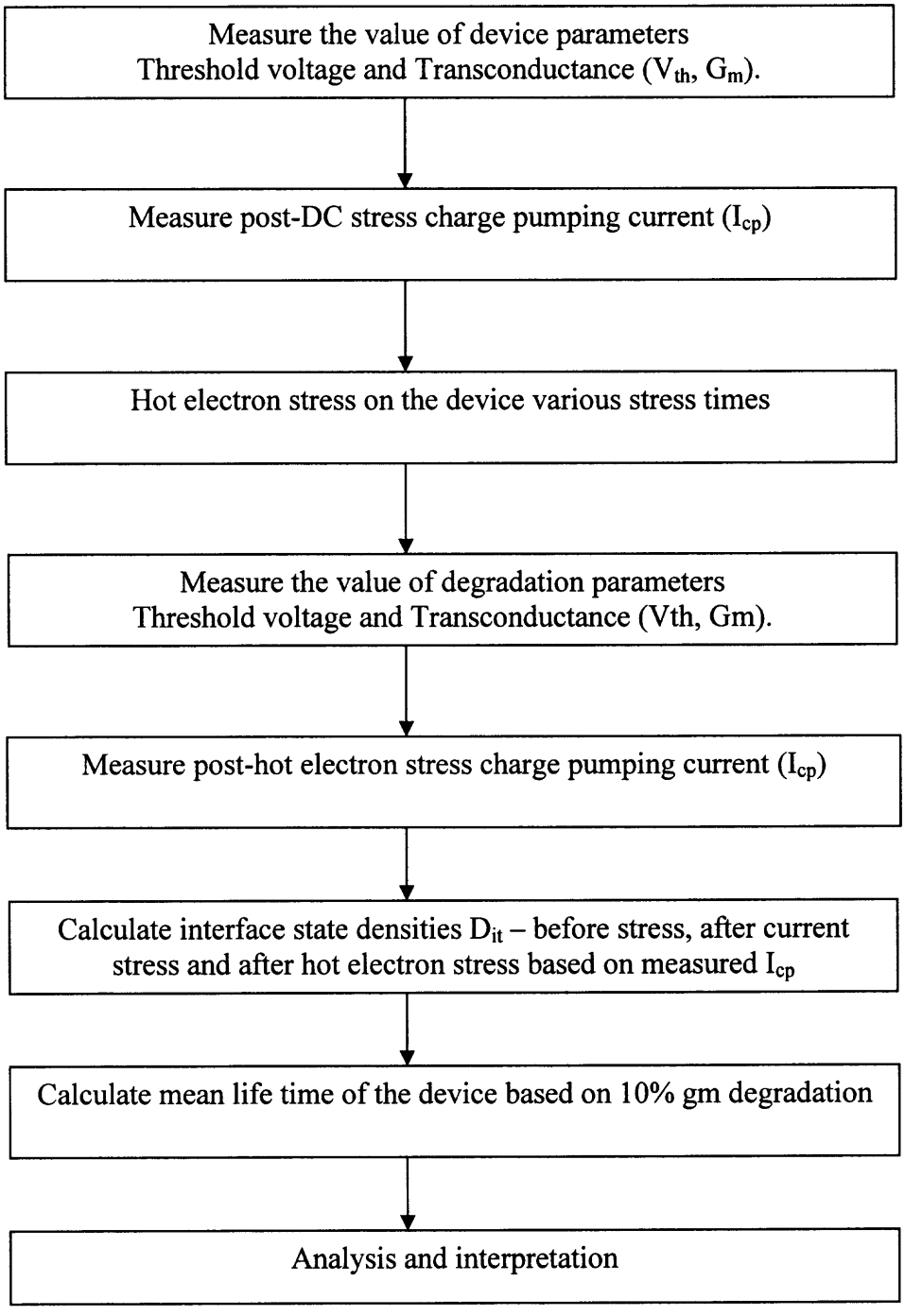
CHAPTER 3

EXPERIMENTAL SETUP

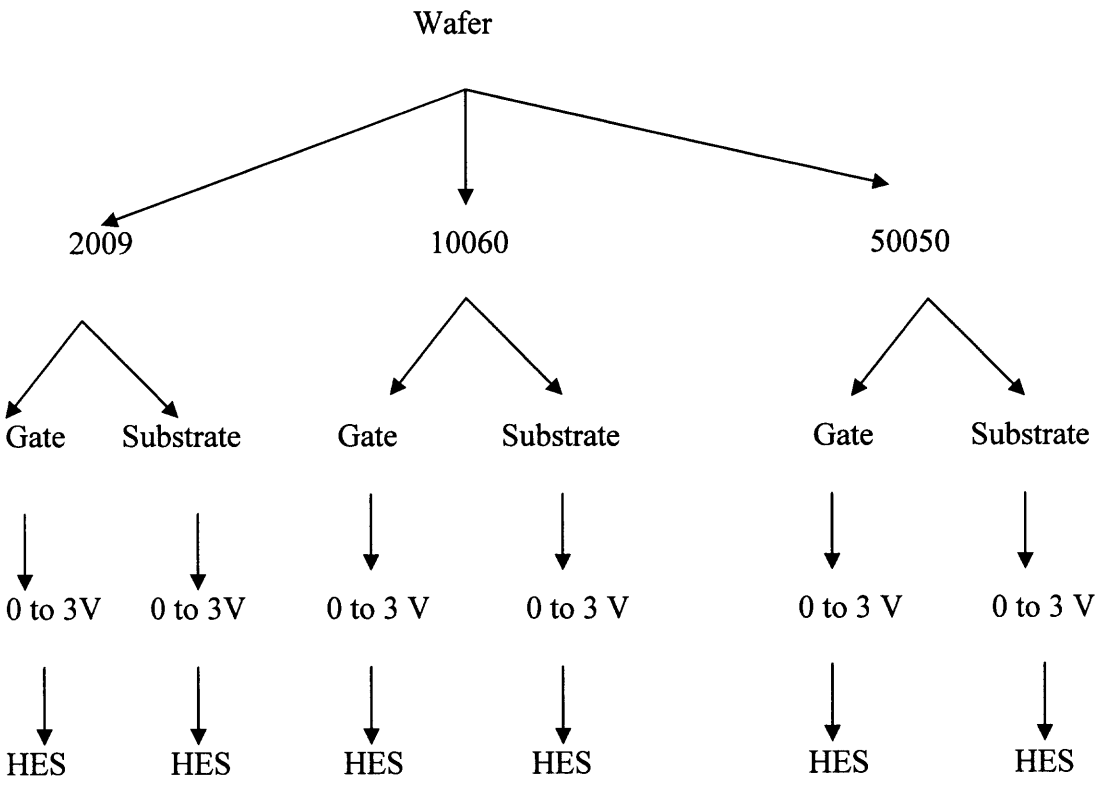
3.1 Measurement Steps

MOSFET devices processed using 0.25 μm technology were used as test devices. Three types of devices based on the nature of pre-existing traps were considered for the stress experiments. Devices parameters (threshold voltage and transconductance) and charge pumping current were measured experimentally based of the setup as explained in following paragraphs. The basic flow in which the stress experiments were conducted is given below in the form of a flowchart.




Measure the value of device parameters
Threshold voltage and Transconductance (V_{th}, G_m).
Measure post-DC stress charge pumping current (I_{cp})
Hot electron stress on the device various stress times
Measure the value of degradation parameters
Threshold voltage and Transconductance (Vth, Gm).
Measure post-hot electron stress charge pumping current (I_{cp})
Calculate interface state densities D_{it} – before stress, after current stress and after hot electron stress based on measured I_{cp}
Calculate mean life time of the device based on 10% gm degradation
Analysis and interpretation

The experiments were classified based on nature of pre-existing traps, nature of injection, nature of stress. The flow in which these experiments and the subsequent measurements that were performed is summarized in the form of tree diagram as below:



The measurements of following parameters are discussed in detail.

3.2 Threshold Voltage and Transconductance (Vt and gm) Measurement

The basic device parameters – threshold voltage V_t and transconductance g_m are being measured on transistors, before and after subjecting them to current stress and hot electron stress. This measurement is done using the GO-NOGO program of HP4156B – Precision Semiconductor Parameter Analyzer. The measurement of threshold voltage and transconductance parameter of a transistor is shown in the Figure 3.1

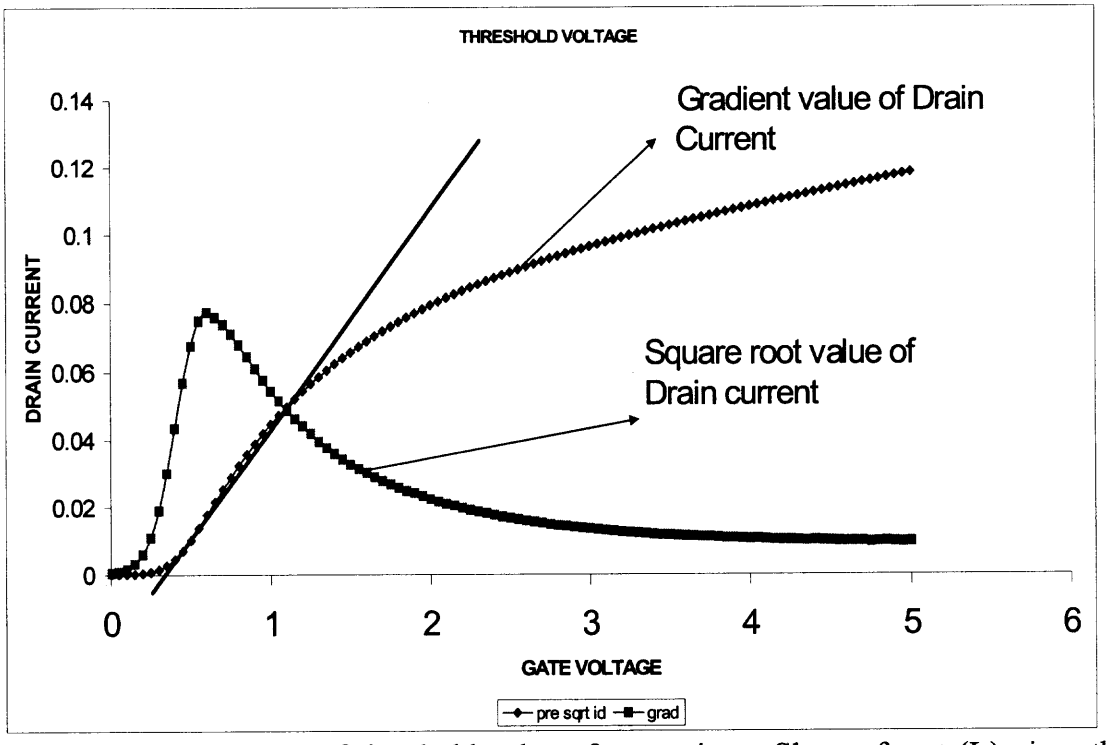


Figure 3.1 Measurement of threshold value of a transistor. Slope of sqrt (I_d) gives the threshold value.

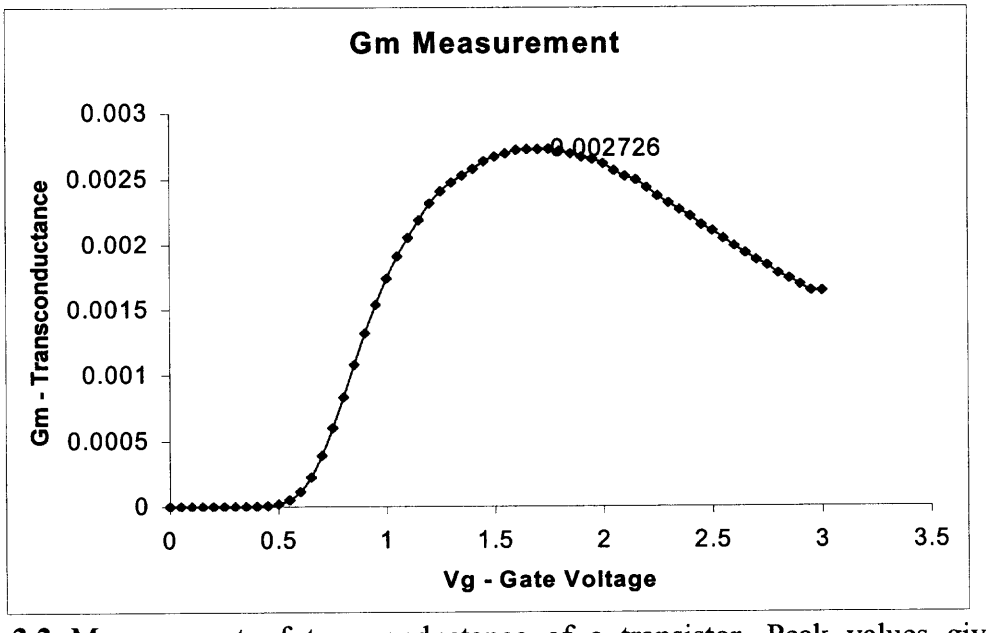


Figure 3.2 Measurement of transconductance of a transistor. Peak values give the transconductance value of the transistor.

3.3 Peak Substrate Current Measurement

In order to inflict maximum damage to the transistor during hot electron stress, the peak gate voltage at which the maximum substrate current occurs needs to be measured. This experiment measures the peak substrate current for various of gate voltages. This is done using I_bVsV_g program. This program measures the substrate current when it sweeps for a range of gate voltage.

3.4 DC Current Stress Measurement

Since the plasma-induced damage is primarily due to electrical charging, the damage to the gate oxide should be identical to that produced by applying a constant current to the gate electrode of an unstressed device for duration equal to the process time. The current necessary to reproduce the plasma-charging damage would correspond to that collected by the antenna during plasma processing. In the experiment, the transistors were subjected to current stress of 10 nA for a period of 3 secs. The polarity of the current stress was based on the type of injection i.e. gate injection or substrate injection. During gate injection, the value is given as -10 nA and was 10 nA during substrate injection. When gate current injection was carried out, the source and drain of the transistor was reverse biased with a potential from 0 V to 3 V. The setup was operated under Lab-View environment as shown in the Figure 3.3. Both types were of F-N injection.

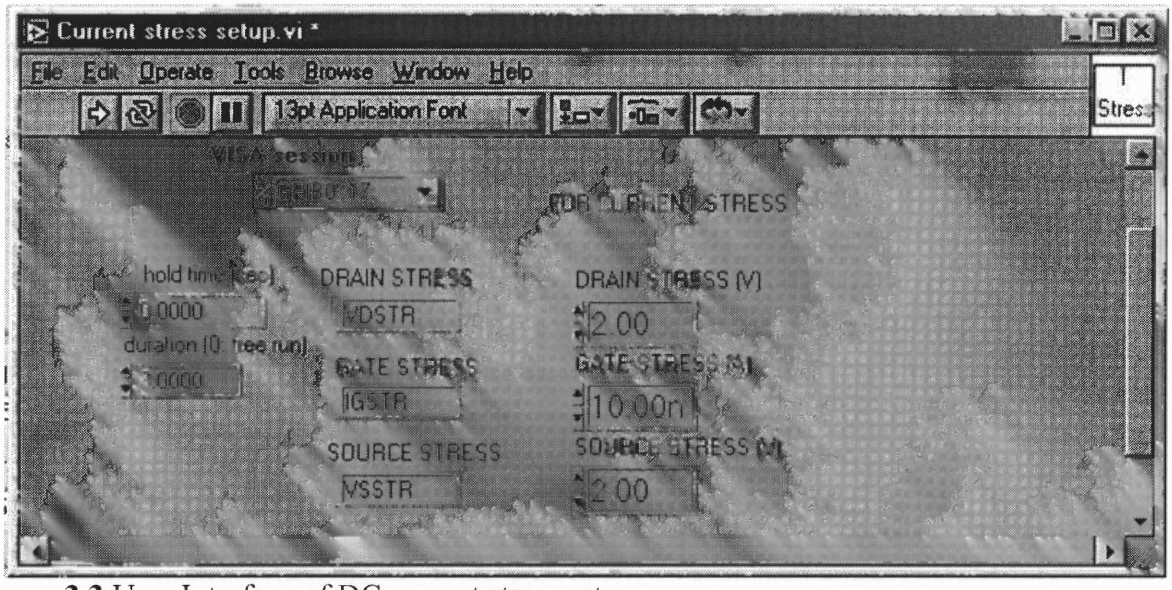


Figure 3.3 User Interface of DC current stress setup.

3.5 Measurement of Interface Traps

The charge pumping principle for MOSFET devices has been successfully applied to characterize the fast interface traps in MOS transistors. This technique is adequate for the evaluation of the type of degradation of MOSFET devices due to hot-carrier injection, Fowler-Nordheim tunneling, radiation damage etc.

3.5.1 Physics of Charge Pumping

In the charge pumping method, the MOSFET is used as a test structure. The method is suitable for interface trap measurements on small-geometry MOSFET's rather than large-diameter MOS capacitors. The source and the drain of the MOSFET are tied together and slightly reverse biased with a voltage V_r. The square wave voltage is applied which has sufficient amplitude for the surface below the gate to be driven into inversion or accumulation (Fig 3.4). The pulse train can also be triangular or trapezoidal.

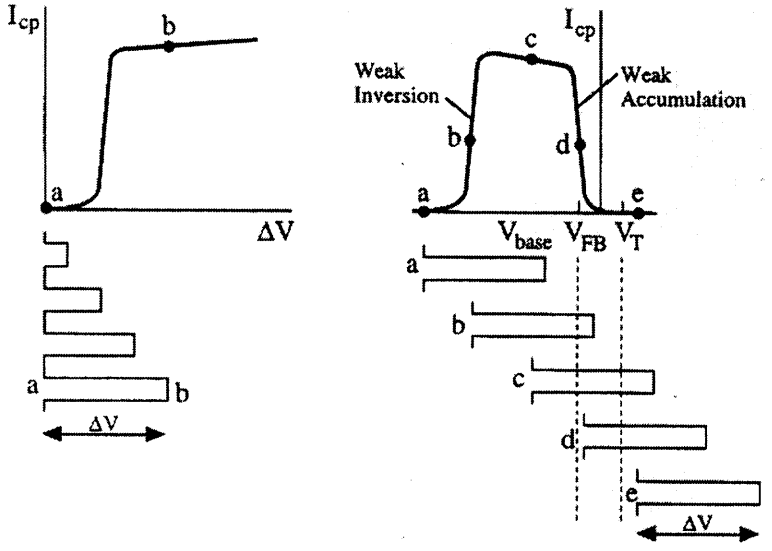


Figure 3.4 Charge pumping principle.

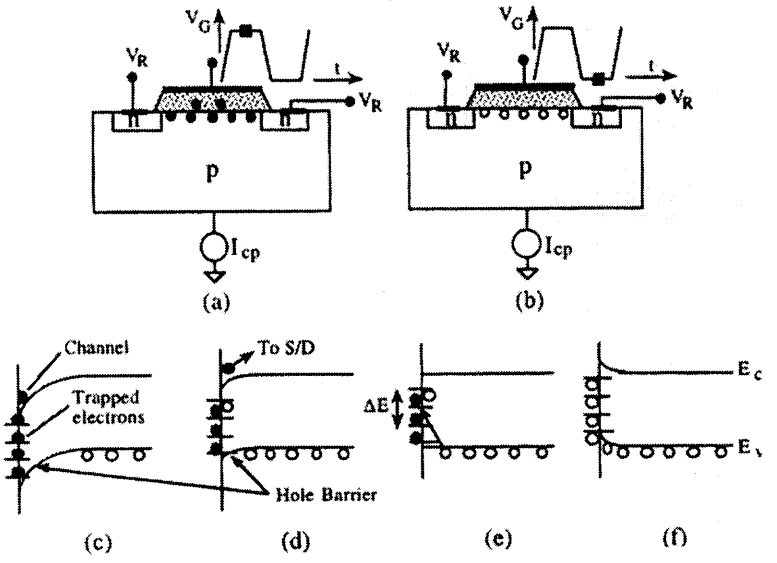


Figure 3.5 Physics of charge pumping.

Consider that the MOSFET is in heavy inversion shown in the Figure 3.5(a) as a result of positive gate voltage. The corresponding semiconductor band diagram from the

Si surface into the substrate is shown in the Figure 3.5(c). The interface traps, continuously distributed through the band gap, are represented by filled circles representing electrons occupying interface traps. When the voltage changes from positive to negative potential, the surface changes from inversion to accumulation and finally ends up as in Figure 3.5(b) and 3.5(f). The important processes take place during the transition from inversion to accumulation and from accumulation to inversion.

When the gate pulse falls from its positive to its negative value during its finite transition time, electrons in the inversion layer drift to both source and drain. In addition, electrons captured by those interface traps near the conduction band are thermally emitted into the conduction band and also drift to source and drain. Those electrons on the interface traps deeper within the band gap do not have sufficient time to be emitted and will remain captured on interface traps. Once the hole barrier is reduced holes flow to the surface where some are captured by those interface traps still filled with the electrons. Holes are indicated by the open circles on the band diagrams. Finally, most traps are filled with holes as shown in the Figure 3.5(f). When the gate returns to its positive voltage, the inverse process begins, and electrons flow into the interface to be captured. For a square wave of frequency f, the time available for electron emission is half the period T_e = ½ f. The energy interval over which the electrons are emitted is from the equation

$$E = kT \ln (\sigma_n \upsilon_{th} N_c / 2f).$$

During the reverse cycle when the surface changes from accumulation to inversion, the opposite process occurs. Holes within an energy interval

$$E - E_v = E = kT \ln (\sigma_p \upsilon_{th} N_v / 2f).$$

are emitted into the valence band, and the remainder combine with the electrons flowing in from source and drain. Those electrons on interface traps within the energy interval ΔE,

$$\Delta E = E_g - kT (\ln (\sigma_n \upsilon_{th} N_c / 2f) + \ln (\sigma_p \upsilon_{th} N_v / 2f)).$$

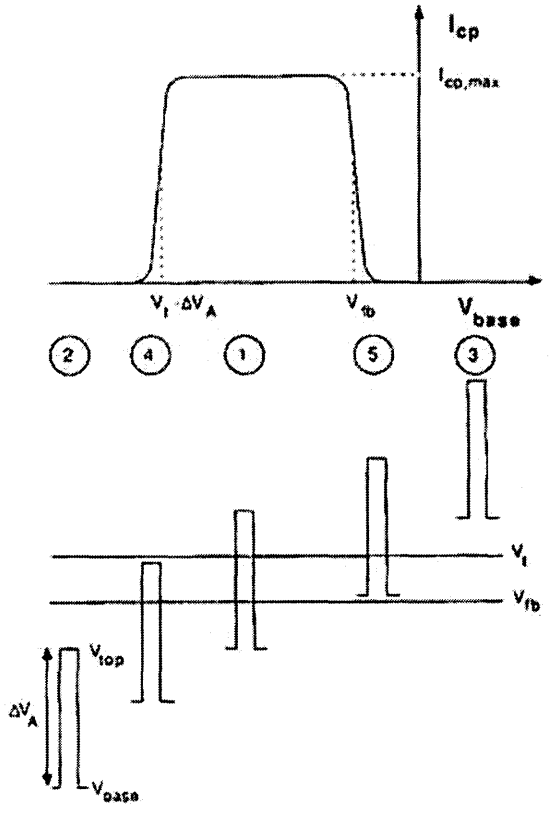
recombine with holes.

Q_n/q electrons/cm^2 flow into the inversion layer from source/drain but only $(Q_n/q - D_{it}/E)$ electrons/cm^2 flowing back into the source/drain. $D_{it} \Delta E$ electrons/cm^2, the difference, recombines with holes. For each electron-hole pair recombination event, an electron and a hole must be supplied. Hence $D_{it} \Delta E$ holes/cm^2 also recombines. In other words, more holes flow into the semiconductor than leave, giving rise to the charge pumping current I_{cp}. The capacitor in parallel with the ammeter averages the ac current to dc current. $D_{it} \Delta E$ holes being supplied at rate of f Hz to a MOSFET with gate area A_g give rise to a current $Icp = q A_g f D_{it} \Delta E$. I_{cp} is in the order of 10^{-8} to 10^{-11} A. I_{cp} has been found to be proportional to both gate area and pump frequency.

The gate of the MOS transistor is connected to the pulse generator and a reverse bias is applied to the source and the drain diodes, while the substrate current is measured. This current is caused by the repetitive recombination at the interface traps of minority carriers coming from the source and the drain with the majority carriers coming from the substrate when the gate pulses the channel between inversion and accumulation. Therefore, the substrate current is directly proportional to the interface state density, the gate area and the frequency of gate pulses.

3.5.2 Description and Analysis of the Charge Pumping Technique

Five operation regions can be distinguished in the behavior of the substrate current as a function of the base level of gate pulses, as illustrated in Figure 3.6



Schematic illustration of the measurement method for the case of an n-channel MOSFET. By changing the pulse base level V_{base} with constant amplitude, five operating regions are distinguished:
1) $V_{base} < V_{fb} < V_t < V_{top}$: normal charge pumping regime;
2) V_{base}, $V_{top} < V_{fb}$: no current measured;
3) V_{base}, $V_{top} > V_t$: no current measured;
4) $V_{base} < V_{fb} < V_{top} < V_t$: transition from zero to maximal current;
5) $V_{fb} < V_{base} < V_t < V_{top}$: transition from maximal to zero current.

Figure 3.6 Regions of operation of MOSFET under charge pumping experiment.

These regions will now be briefly discussed.

REGION 1 ($I_{cp} = I_{cp\,max}$): When the base level (V_{base}) is lower than the flatband voltage (V_{fb}) while the top level of the pulse (V_{top}) is higher than the threshold voltage (V_t), the conventional charge pumping effect occurs. This means that a net amount of charge is

pumped from the source and the drain to the substrate via the fast interface traps each time the transistor is pulsed from inversion toward accumulation and back.

REGION 2 & 3 ($I_{cp} = 0$) : In region 2, the top and base levels of the gate pulse train are below the flat-band voltage. Therefore, the fast interface traps are permanently filled with holes and consequently no recombination current is measured. In region 3, the channel is permanently in inversion, so no holes reach the surface at any time. For both the cases, the measured substrate current consists of only the source and drain leakage currents.

REGION 4 & 5 ($0 < I_{cp} < I_{cpmax}$): In region 4, the charge pumping current increases from 0 to a saturation level. The recombination process disappears when going from region 1 to region 2 because the electron concentration at the interface during the inversion part drastically reduces when the top level does not reach V_t. Therefore the rising edge of the charge pumping current I_{cp} Vs. base characteristic is located at $V_t - \Delta V_a$, where ΔV_a is the amplitude of the gate pulse. Therefore the transition zone is determined by the recombination process in weak inversion.

3.5.3 Charge Pumping Current Measurement

The measurement was carried out based on the test setup as shown in the Figure 3.7.

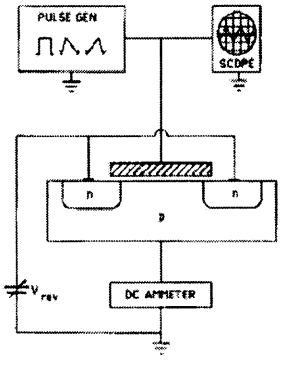


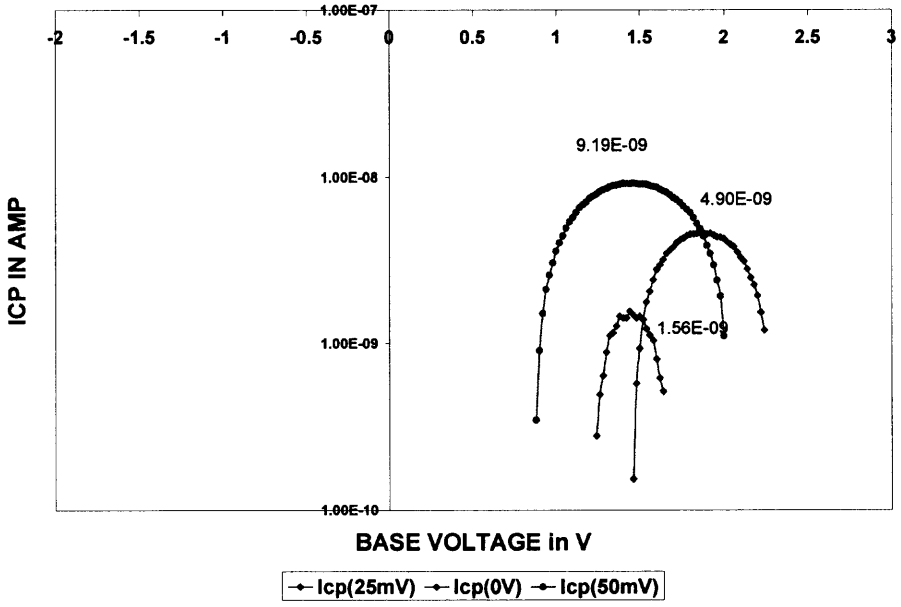
Figure 3.7 Charge pumping setup.

Charge pumping experiment

1. Short the drain and source of the transistor or apply small reverse bias voltage.
2. Apply a varying pulse base width (using HP 8013B pulse generator) at the gate (Sweep the gate voltage) - DC bias superimposed on a pulse.
3. Adjust the value of the frequency > 10 KHz.
4. Make sure that the pulse height and pulse width are to the required levels (no less than 0.5 V and no greater than 3 V)
5. Measure the current at the substrate which gives the charge pumping current.
6. Plot the current with respect to the gate bias voltage.

The charge pumping current varies based on the settings. Various values of pulse width, pulse amplitude, frequency and reverse biasing were done and the results are summarised as follows:

3.5.4 Effect of Reverse Bias Voltage of Source/ Drain on Charge Pumping Current

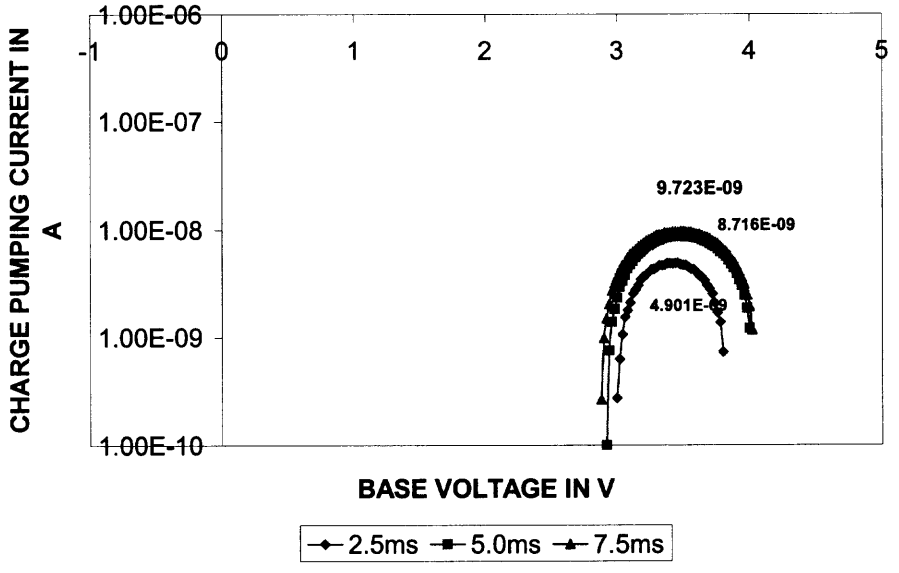


SETTINGS: PULSE AMP = 300 mV; Freq. = 50 MHz

Figure 3.8 Charge pumping current for various reverse bias voltage values applied.

The reverse bias at the source and drain affects the threshold voltage level limiting the scanning into the source and drain regions of the transistor. Hence it decreases the maximum charge pumping current as the reverse bias voltage is increased.

3.5.5 Effect of Pulse Width on Charge Pumping Current

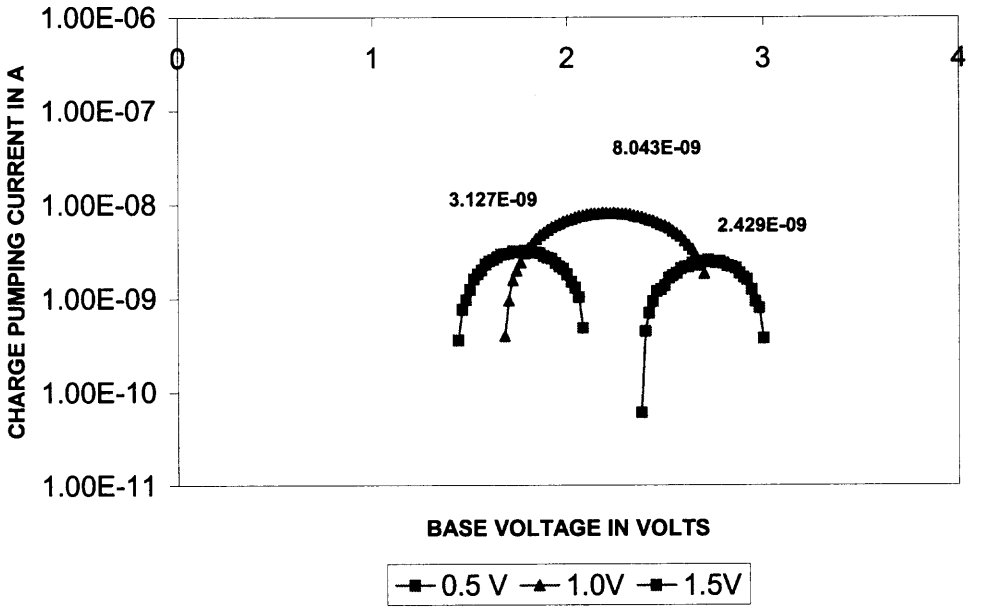


SETTINGS: FREQ = 50 MHz; REVERSE BIAS VOLTAGE : 50 mV

Figure 3.9 Charge pumping current values for various pulse widths.

Fig 3.9 explains the effect of pulse width on the charge pumping current of the transistor. The time at which the top and the base levels of pulse change, influencing the threshold voltage level of the transistor. This varies the recombination current of holes and electrons, affecting the charge pumping current. When the pulse width is smaller, the recombination current is significantly less due to which there is an increased charge pumping current.

3.5.6 Effect of Pulse Amplitude on Charge Pumping Current



SETTINGS: PULSE AMPLITUDE : 2 V, REVERSE BIAS VOLTAGE : 50 mV

Figure 3.10 Charge pumping current values for various pulse amplitude values.

From Figure 3.10 it is seen that the effect of increasing the pulse amplitude is two-fold. Increasing the amplitude of the pulse allows to sense interface traps further into the source and the drain regions, due to which there is a tailing effect. Also, the charge pumping current increases with increasing pulse amplitude, since the distance from the source and channel junction increases with increasing amplitude.

3.5.7 Effect of High Field Injection and Hot Electron Injection on Charge Pumping Current

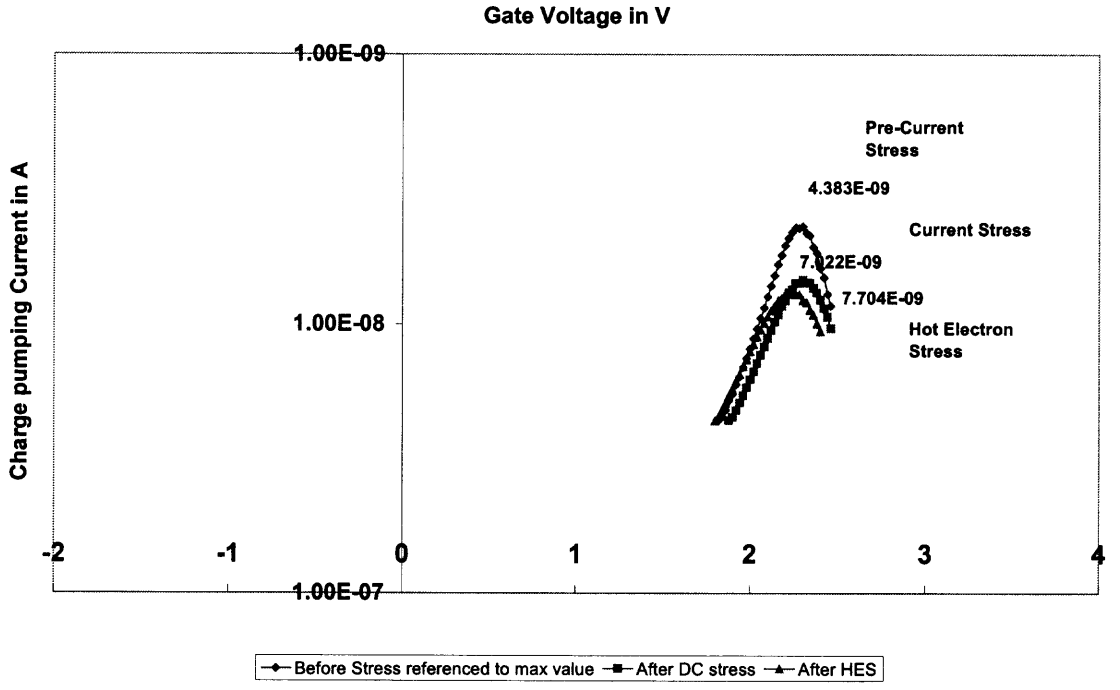


Figure 3.11 Charge pumping current under application of stress.

Fig 3.11 explains the effect on the charge pumping current after the application of current and hot electron stress. Since DC stress and hot electron stress on the transistor create interface traps, the charge pumping current increases. It is known that the charge pumping current signifies the amount of interface traps present at the interface of the transistor.

3.6 Hot Electron Stress Measurement

The basic flow for hot electron stress measurement is given below:

1. Find the threshold voltage V_{th} and transconductance g_m of the transistor

2. Determine the drain stress bias voltage – V_{dstr} – I_dV_d measurement to find the maximum voltage to be applied at the drain. The general rule is that the value of this voltage is half or less than half of V_{dd}. In this case, $V_{dd} = 3.3$ V and $V_{d\,str} = 1.65$ V.

voltage at the gate to be applied.

4. Set this to be the gate and the drain voltage for the stress.

5. Using this condition repeat the experiment for different values of stress time – 1 , 2 , 3.16 , 10, 31.6 , 100, 316.2, 1000, 1200 secs.

6. Calculate the change in transconductance (Δg_m) and change in threshold voltage (ΔV_{th}).

This setup was operated under Lab View environment as shown in the Figure 3.12.

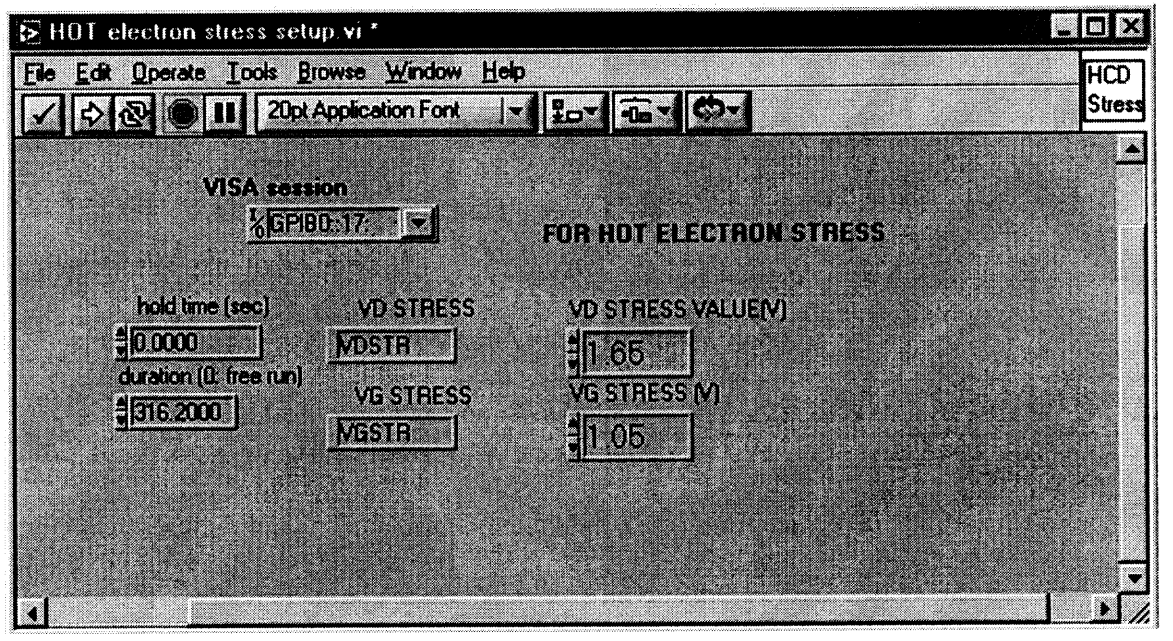


Figure 3.12 User interface of hot electron stress setup.

3.7 Estimation of Interface State Density D_{it}

The interface state density (D_{it}) can be calculated from the measured charge pumping current using the formula

$$D_{it} = I_{cp} / f * q * A_g * kT$$

Where

f – Frequency of operation

q – Electronic charge -> 1.6 x 10^{-19}C

A_g – Channel Area in cm^2

kT- Thermal Energy – 0.026 eV

In all the cases, the frequency of operation was 1 MHz. The channel area was calculated from width W and length L of the transistor and is found to be 10^{-2} cm x $3.5x10^{-5}$ cm = $3.5x10^{-7}$ cm^{-2}.

In all the measurements, the peak value of interface state density was considered. A typical graph showing the values of interface state density is given below:

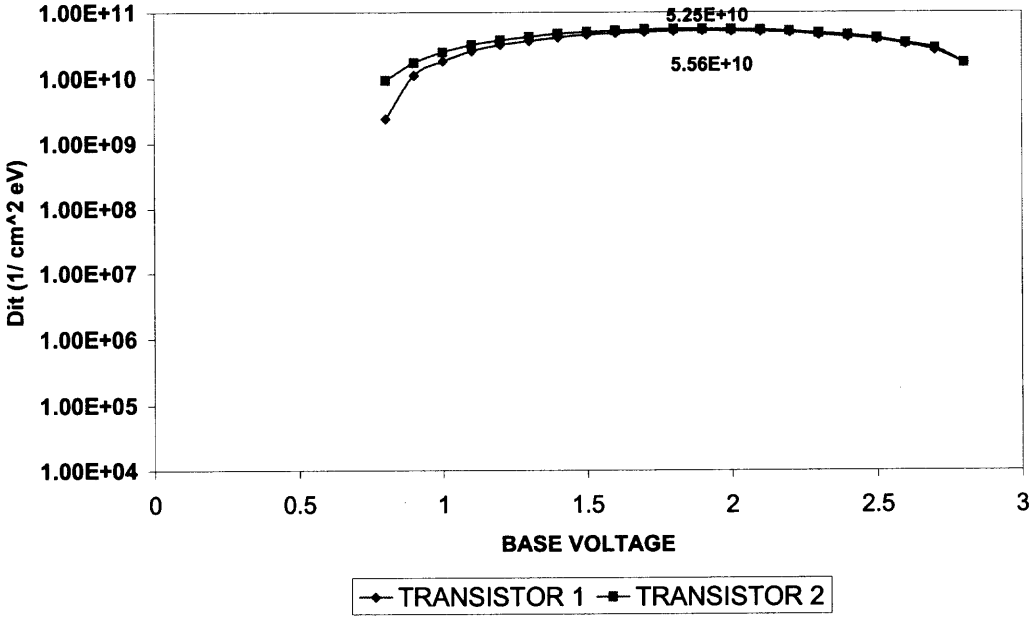


Figure 3.13 Calculation of interface state density.

3.8 Estimation of Hot Carrier Lifetime

Hot carrier lifetime is defined as the time that the transistor takes to degrade to 10% from its initial transconductance g_m value. The lifetime is estimated by extrapolating the values

of g_m obtained during hot electron stress for 10% of its original value. A typical graph calculating the life time of hot carriers is shown in the Figure 3.14.

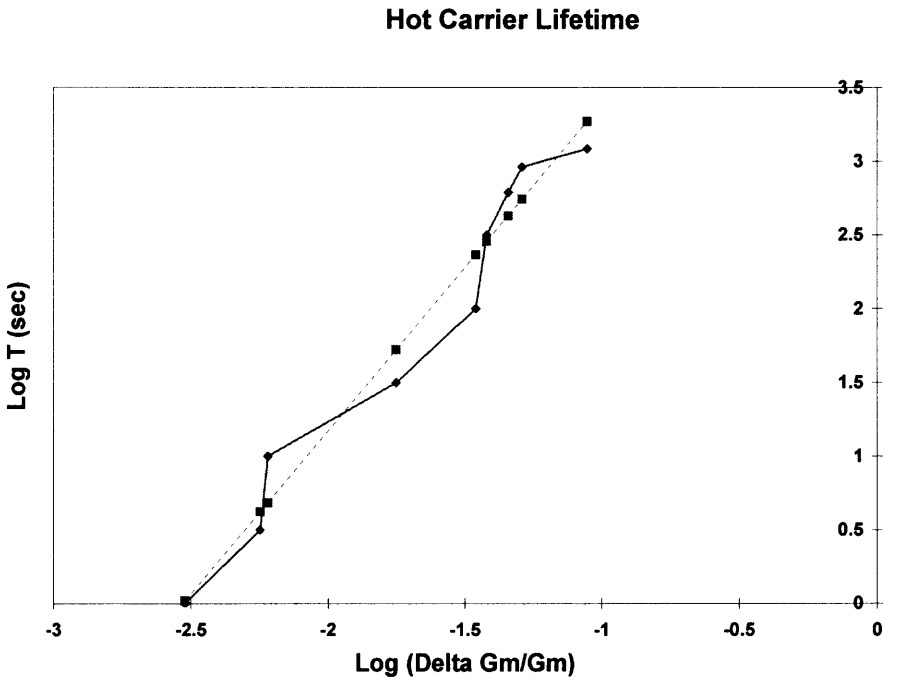


Figure 3.14 Calculation of hot carrier life time of a transistor.

The corresponding graph is given below

Time in secs	Gm values	Del gm/gm	Log time		y=mx +c
0	2.657			54.58416	
1	2.649	0.003011	0	0.279907	0.444255
3.16	2.642	0.005645	0.499687		0.58806
10	2.641	0.006022	1		0.608604
31.6	2.61	0.017689	1.499687		1.245453
100	2.565	0.034626	2		2.169912
316.23	2.556	0.038013	2.500003		2.354804
615.9	2.536	0.04554	2.78951		2.765674
915.59	2.521	0.051186	2.961701		3.073827
1220	2.422	0.088446	3.08636		5.107636
		0.1			5.738323

Antilog of the above value (5.738323) gives the hot carrier life time.

3.9 NMOS Devices and Current Stress

The wafers studied consisted of nMOS transistors processed using 0.25 μm CMOS technology. Transistors had a channel area of 0.35 μm^2 and thickness of the gate oxide was 6 nm. Threshold voltage and transconductance values measured before stress were quite uniform. The schematic in Figure 3.15(a) shows a typical injection mode used to evaluate the oxide integrity where all the terminals are connected together to form a common ground. Transistors with three types of antenna ratios 2009:1, 10060:1 and 50050:1 were subjected to about 30 mA/cm^2 constant current stresses for 3 secs using gate injection and substrate injection mode. Screening effect at the junctions were studied by applying voltages of 0 V, 1 V, 1.5 V, 2 V and 3 V at the source and the drain using a set up described in Figure 3.15(b). These voltages were chosen inorder to simulate the plasma voltages that could possibly get generated during the plasma processing conditions. Following the current stress the devices were subjected to hot carrier aging stress using maximum substrate current. The interface trap density D_{it} was measured before and after the high field injection and after the hot electron stress by measuring the charge pumping current I_{cp} using the charge pumping technique. Each type of stress measurement was done on a separate group of devices. The values that degrade due to the stress, namely, threshold voltage V_t and transconductance g_m were obtained using a HP4156 Precision Semiconductor Parameter Analyzer setup operated under an automated Lab View environment.

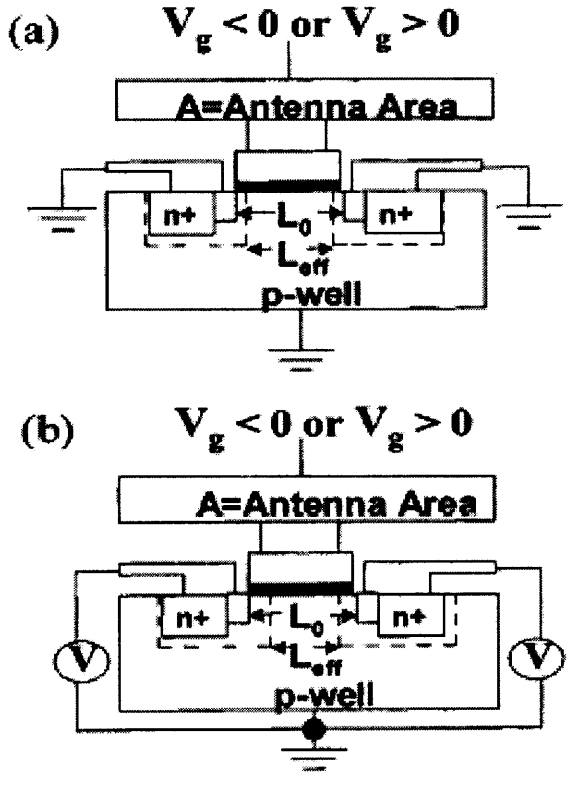


Figure 3.15 The cross-sectional view of n-MOSFET (a) in a stressing condition (b) with source and drain at a screening potential.

CHAPTER 4

STRESS INDUCED INTERFACE STATES

4.1 Threshold Voltage Degradation

Figure 4.1 shows the variation in threshold voltage, V_t immediately after the current stress at different conditions for gate and substrate injection. It is clearly seen that there is reduced device degradation around 1.5 to 2 V. This suggests that oxide charges trapped in the bulk may recombine with the opposite charges, improving the flatband voltage.

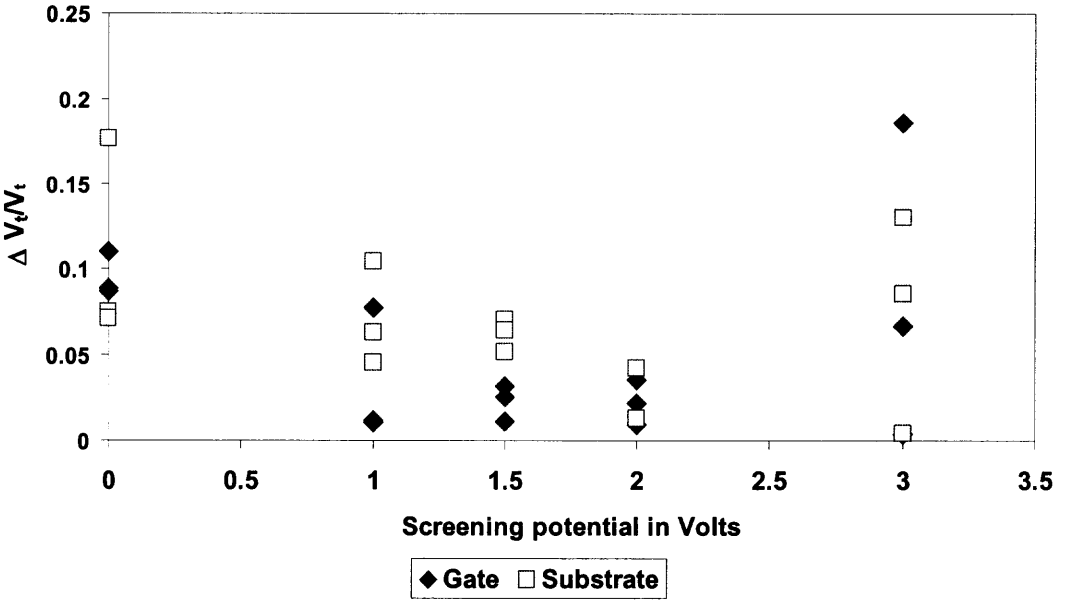


Figure 4.1 Threshold V_t and Transconductance g_m degradation.

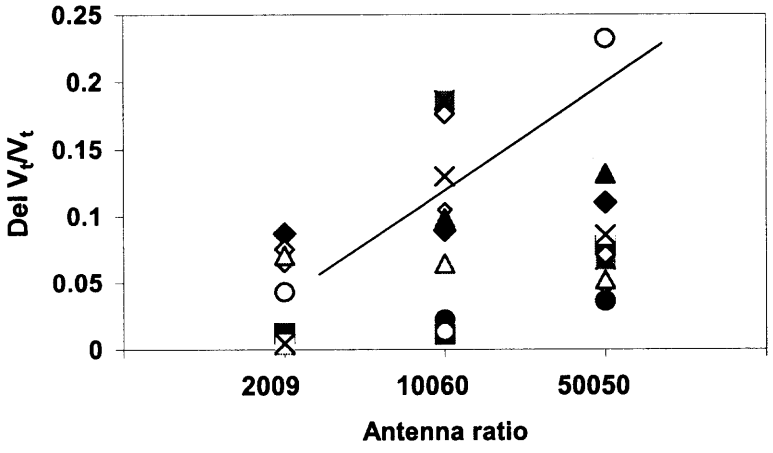


Figure 4.2 Variation in threshold voltage for various groups of devices. Dark spots refer to gate type injection and light spots refer to substrate type injection.

Figure 4.2 shows the variation in threshold voltage, V_t immediately after the current stress at different conditions for various antenna ratios. The latent damage in larger antenna ratio shows an increased spread of V_t shift after stress. There is an increase in V_t after current stress suggesting an enhanced electron trapping in the oxide for devices with larger antenna ratio. It is expected because devices with larger antenna ratios are damaged more due to exposure to plasma processing. It is known that plasma damaged devices have higher concentration of electron traps in the oxide.

4.2 Transconductance Degradation

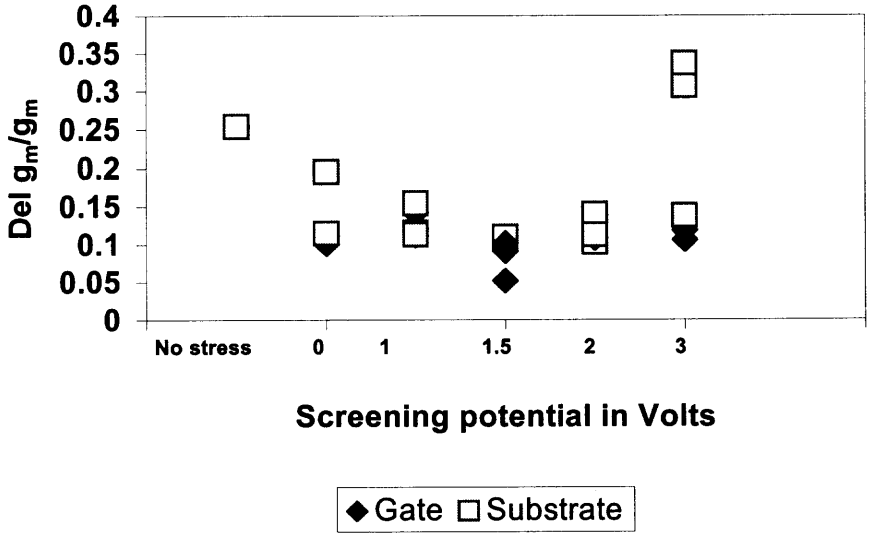


Figure 4.3 Transconductance degradation of transistors subjected to gate and substrate injection.

Figure 4.3 shows the g_m degradation for all groups of transistors, immediately after the devices were subjected to current stress. The transconductance degradation for devices of gate injection is minimum when the screening potential is around 1.5 V. At lower screening potential, it is seen that the transconductance degradation is high due to ineffective screening of the drain and the source edges.

Also note that the degradation is maximum at the near-breakdown potential. The same argument may be applied for the devices subjected to substrate injection. The damage is again approximately low at 1.5 – 2.0 V.

4.3 Interface State Density D_{it}

4.3.1 Gate Injection

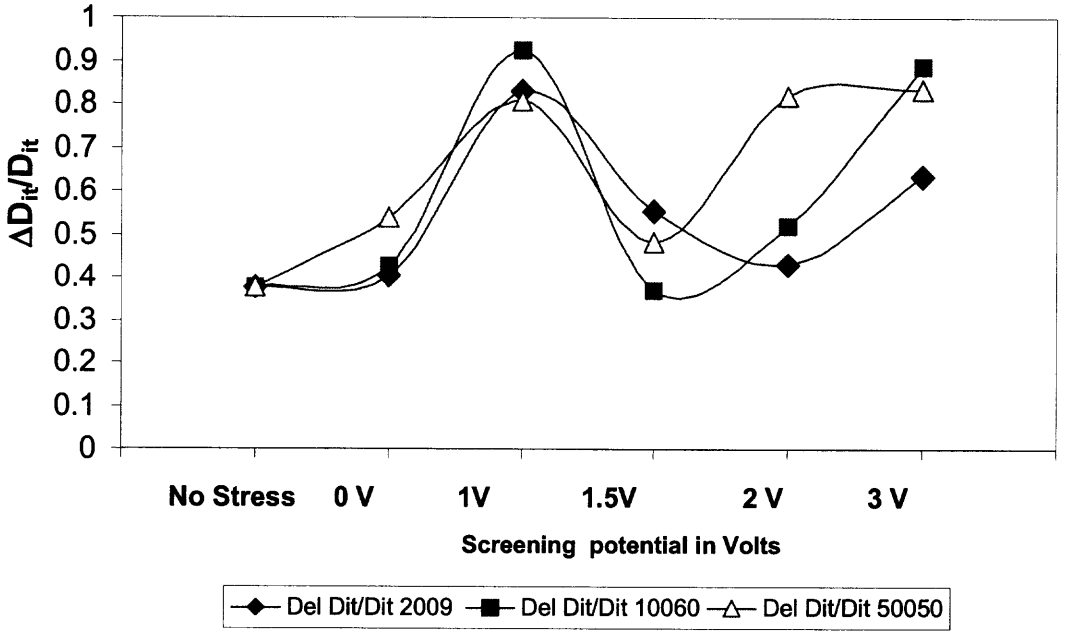


Figure 4.4 Variation in interface state density of all the three antenna ratios for various screening potentials for first set of experiments.

Figure 4.4 and Figure 4.5 shows the variation in interface state density, measured by charge pumping experiment, of various transistors after being exposed to a current stress with the applied screening potential under gate injection and a subsequent hot carrier stress for two groups of devices respectively. It is seen that the screening effect is prominent for a wider range of screening voltage for transistors with the smallest antenna ratio (2009) and most effective (lowest D_{it}) at 2 V approximately. The most effective screening potential gradually decreases, as the antenna ratio becomes larger. For antenna ratios 10060 and 50050 the most effective screening potentials are 1.7 V and 1.5 V respectively. D_{it} at these screening potentials goes through a significant reduction compared to lower voltages. Considering that the doping concentration of the n^+ region of the drain and the channel is constant, the lateral depletion width will vary accordingly to

screen the source and drain edges.

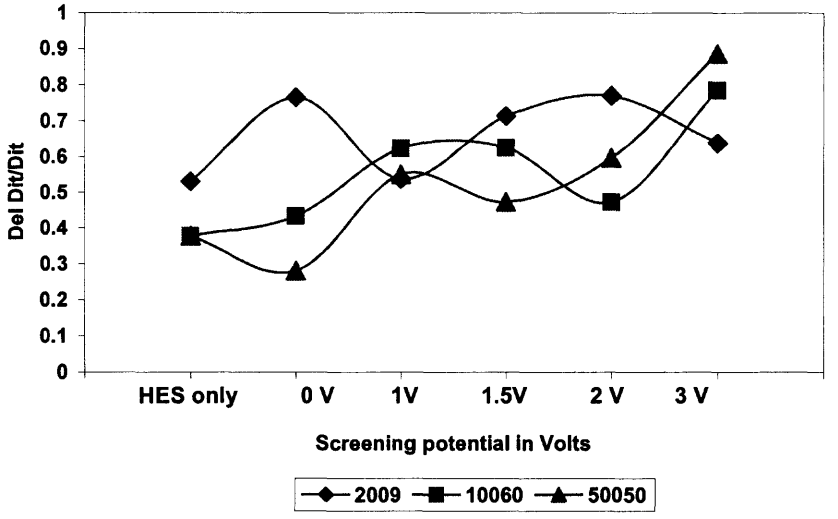


Figure 4.5 Variation in interface state density of all the three antenna ratios for various screening potentials for second set of experiments.

At lower potential the depletion width is not significant enough to screen the drain edge whereas at higher screening potentials the field reaches a near-breakdown of the oxide. This near-breakdown potential causes an increase in D_{it} and the trapped charges near the drain edges. Below this breakdown potential, the channel is effectively screened reducing the interface states. For a larger antenna ratio, the near-breakdown screening potential is comparatively low, because the transistors have pre-existing charges trapped at the interface. The noticeable increase in D_{it} at lower screening potentials that does not screen the drain/source edges effectively (around 1V), is believed to be due to field-enhanced degradation.

4.3.2 Substrate Injection

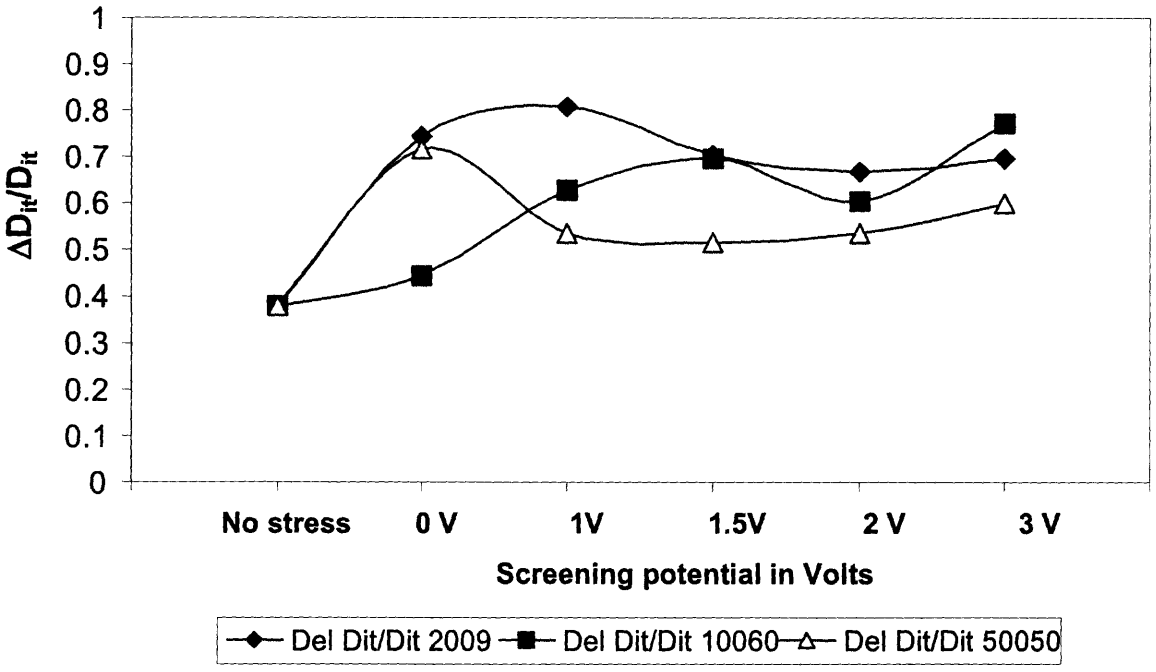


Figure 4.6 Variation in interface state density of all the three antenna ratios for various screening potentials for substrate injection for first set of experiments.

For substrate injection as shown in Figure 4.6 and Figure 4.7, it is seen that the interface state density D_{it} decreases approximately for the same potentials as in the gate injection. For antenna ratios 2009, 10060 and 50050 the most effective screening potentials are approximately 2.1 V, 2.0 V and 1.5 V respectively. The minimal increase of the most effective screening potentials compared to gate injection is mainly due to the injection of thermally generated electrons from the substrate. In the case of gate injection, on the other hand, more electrons are available at the poly Si-SiO_2 interface as compared to substrate injection. The lower screening potential that causes an increase in interface states remains around 1.0 V identical to gate injection.

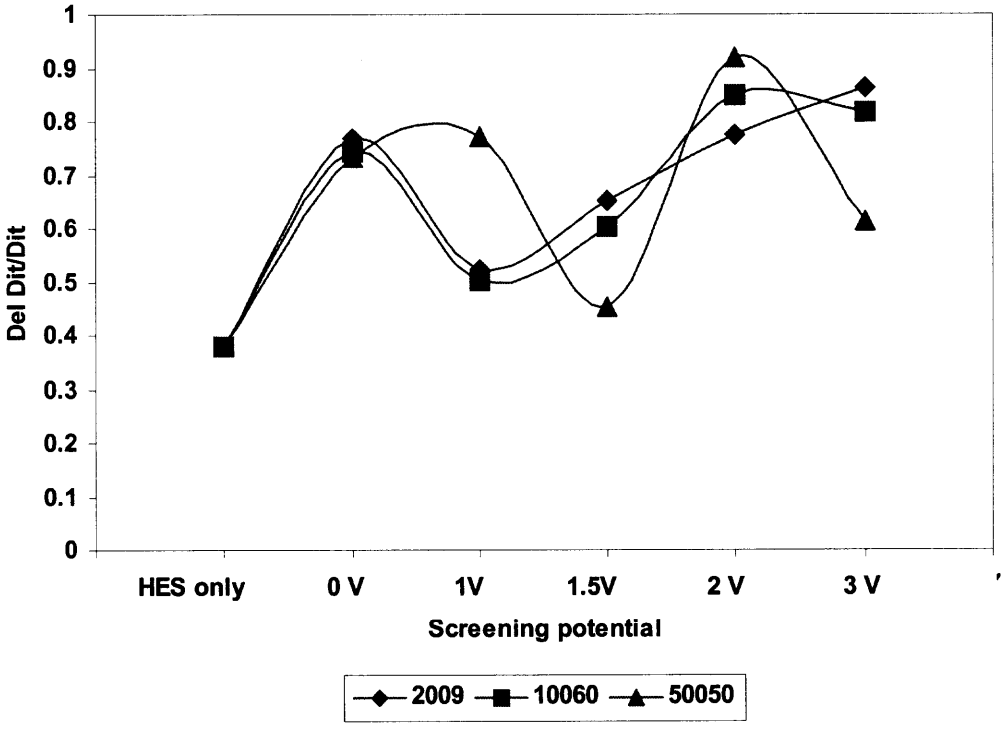


Figure 4.7 Variation in interface state density of all the three antenna ratios for various screening potentials for substrate injection for second set of experiments.

4.4. Hot Carrier Lifetime

4.4.1 Hot Carrier Lifetime for Gate Injection

Figure 4.8 shows the hot carrier lifetime of transistors estimated by transconductance degradation. The hot carrier aging was performed after the transistors were subjected to gate injection under different screening potentials for all the three types of antenna ratios. It is seen that the hot carrier lifetime of these transistors varies almost in accordance with the interface states generated.

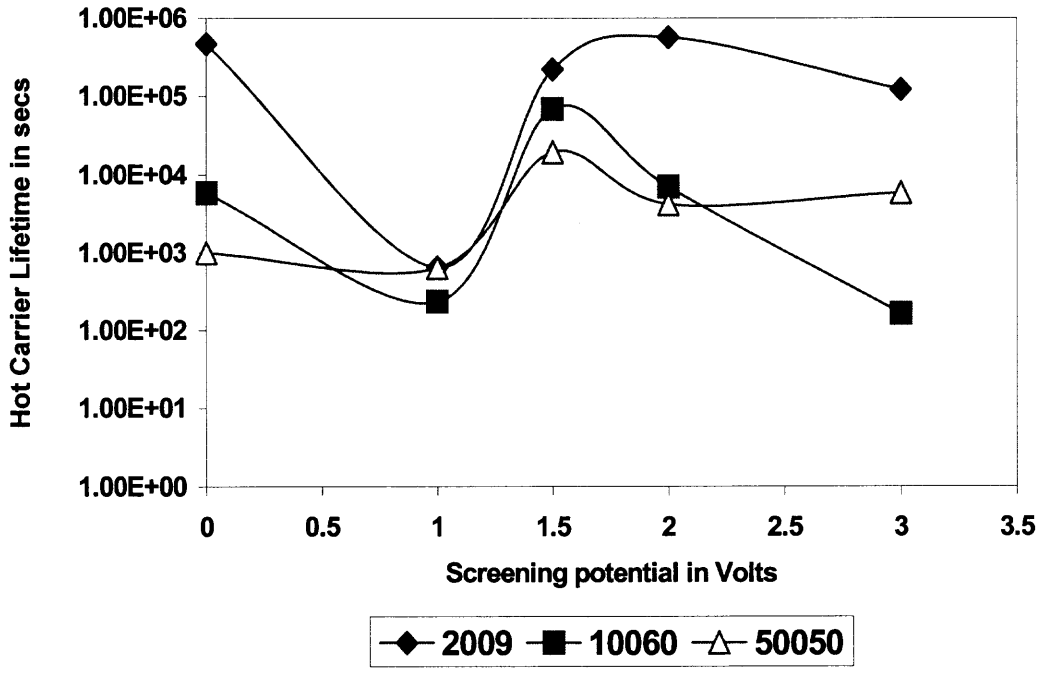


Figure 4.8 Hot carrier lifetime of transistors for gate injection.

A small fraction of hot electrons at the drain edge create damage at the Si-SiO_2 interface, which manifests itself as an increase in interface state density D_{it} and yet another small fraction become trapped in the oxide. Once the device is degraded by the current stress, the hot carrier lifetime goes down as the hot electrons typically fill the traps created during the current stress. However, if the drain edges are screened during the current stress the hot carrier lifetime improves. Since the hot carrier lifetime characteristics, as a function of screening potential, follow the interface state characteristics, it further conforms that at certain screening potentials the drain edges are effectively screened from the damage induced by the current stress.

4.4.2 Hot Carrier Lifetime for Substrate Injection

In the case of substrate injection, as shown in Figure 4.9, the lifetime is maximum when the screening potential is approximately at 1.5 V, which is nearly in accordance with the number of interface states created as referred in Figure 4.6 and 4.7. Also in this case, the transistors with larger antenna ratio suffer maximum damage. It is also noticed that the hot carrier life time of these devices are an order of magnitude lower when compared to the devices subjected to gate injection, indicating strongly that substrate injection is more damaging.

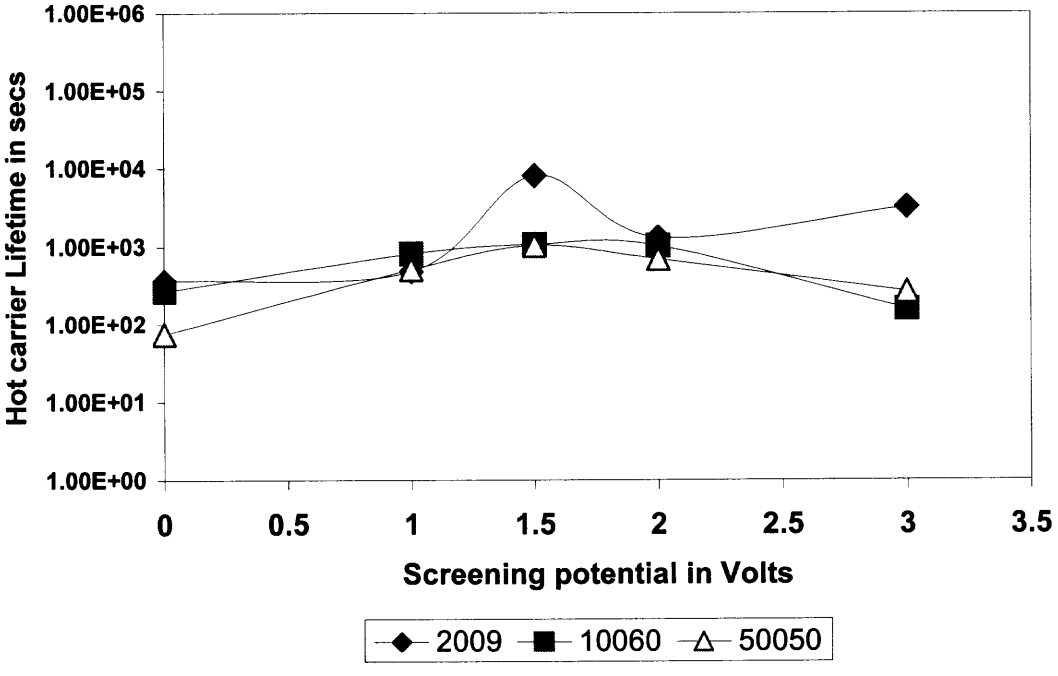


Figure 4.9 Hot carrier lifetime of transistors subjected to substrate injection.

CHAPTER 5

STRESS INDUCED Si-H BOND CONCENTRATION

5.1 Theoretical Background on Si-H Bond Concentration

Hydrogen plays a critical role in the fabrication of high quality Si-SiO_2 interface where the dangling bonds are compensated by hydrogen atoms. The trap formation at Si-SiO_2 interface is an electrochemical process where the hydrogen of Si-H bonds is released and the appearing Si dangling bonds represent interface traps. Interface state density D_{it} is proportional to the concentration of silicon dangling bonds at the interface N-n where N is the total concentration of Si bonds which appear as dangling bonds and n is the concentration of Si-H bonds at the interface.

5.2 Estimation of Si-H Bond Concentration

The concentration of Si-H bonds are estimated based on a simple power law and kinetic equation

$$N_{it} - N_{it0} = n_o / (1 + (kt)^{-\alpha})$$

Where N_{it} and N_{it0} are final and initial interface state densities, n_o is the initial concentration of Si-H bonds for the time dependence trap generation t, k is the reaction constant and α is a constant. It is also noted that $\alpha > 0.5$ for negative gate biases and $\alpha < 0.5$ for positive biases. Evaluation of the reaction constant k is based on the nature of the stress i.e. DC stress or hot carrier stress. Reaction constant k is given by the formula

$k = k_0 \exp(-\varepsilon_a/k_BT)$ for high field injection and

$k = k_o \exp(-\varepsilon_a/k_BT)k_H$ for hot carrier degradation, where

$k_H = 1 + \delta_{HC}|I_{HC}|^{\rho HC}$

Expression for ε_a is evaluated based on the formula

$\varepsilon_a = \varepsilon_{a0} + \beta . k_B T \ln (N_{it}/N_{it0})$ for high field and

$\varepsilon_a = \varepsilon_{a0} + \delta |F|^{\rho} + \beta * k_B T \ln (N_{it}/N_{it0})$ for hot carrier injection.

Prefactor β is approximately assumed to be less than twice of α for high field injection while it is evaluated to be $\beta = 1 + \beta_{\perp} F_{\perp}$ where $F_{\perp}$ is the polarity dependent perpendicular component of the electric field at the interface for hot carrier stress and δ, ρ are fitting parameters. Extracted values of $\beta = 0.6$ for negative gate bias, 1.2 for positive bias, 1.23 for hot carrier stress, $k_H = 1.006$, $I_{HC} = 10$ nA, $\delta |F|^{\rho} = 0.245$ were calculated from experiments while the values of $k = 8 \text{ X } 10^{-10}$ sec^{-1}, $\delta = 1.95 \text{ X } 10^{-3}$ (V/cm) $^{-\rho}$, $\rho = 0.33$, $\delta_{HC} = 6.0 \text{ X } 10^5$ (A/cm^2), and $\rho_{HC} = 1$ were used in the above calculations. All calculations were based on the room temperature 300K. Activation energy (ε_{a0}) of 2 eV that dissociates hydrogen from the interface was used in our estimation.

5.3. Si-H Bond Concentration after Current Stress

5.3.1 Gate Injection

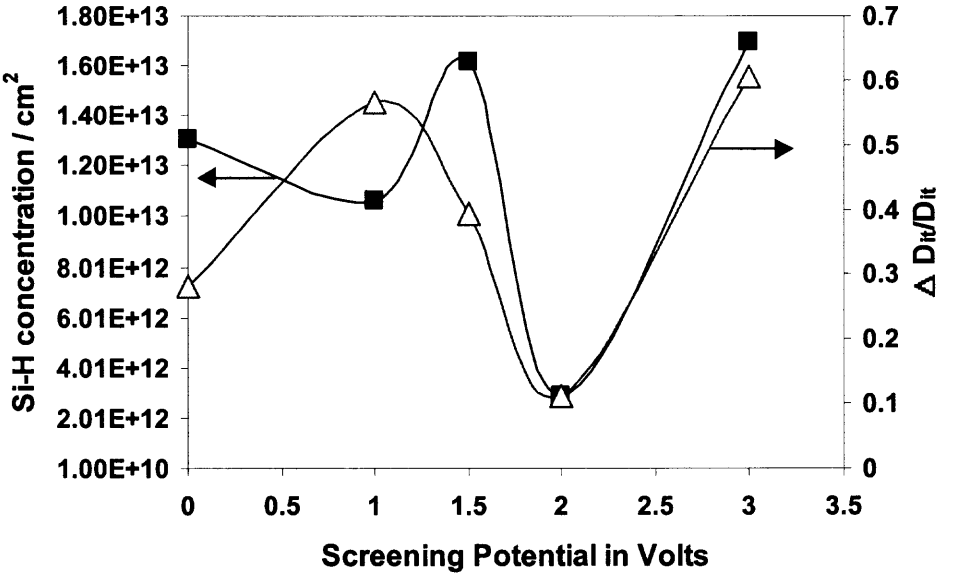


Figure 5.1 Concentration of Si-H bonds for gate injection after DC stress.

Figure 5.1 shows the concentration of Si-H bonds along with $\Delta D_{it}/D_{it}$ as a function of screening potential immediately after the DC stress for gate injection. As per $\Delta D_{it}/D_{it}$, effective screening potential is found to be in the order of 1.5 V to 2 V for gate injection. During the negative current stress (gate injection), electron-hole pairs are being generated at the Si-SiO_2 interface (anode), which react with Si-H bonds. In this reaction, hydrogen (H: atom and H^+: ion) is released breaking the Si-H bonds creating interface traps as described in the following equation.

$$Si\text{-}H + H^+ + e^- \rightarrow Si^* + H_2 \qquad (or) \qquad Si\text{-}H + H \rightarrow Si^* + H_2$$

where Si* represents the dangling Si bond. It is seen that under effective screening, when D_{it} reduces, the Si-H bond concentration increases. Therefore, D_{it} is strongly related to Si-H bond breaking during gate injection. Similar trends were noticed for other groups of

transistors with antenna ratios, 10060 and 50050. Figure 4.2 and Figure 4.3 plot the concentration of Si-H bonds with $\Delta D_{it}/D_{it}$ as a function of screening potential for the antenna ratios 10060 and 50050 respectively.

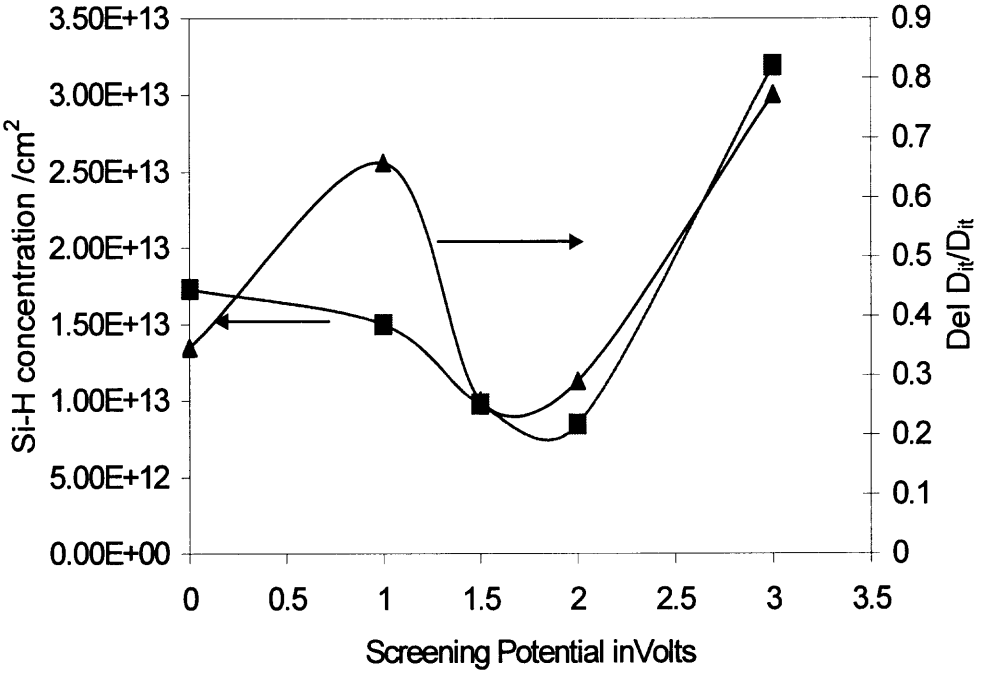


Figure 5.2 Concentration of Si-H bonds for gate injection after DC stress for antenna ratio 10060.

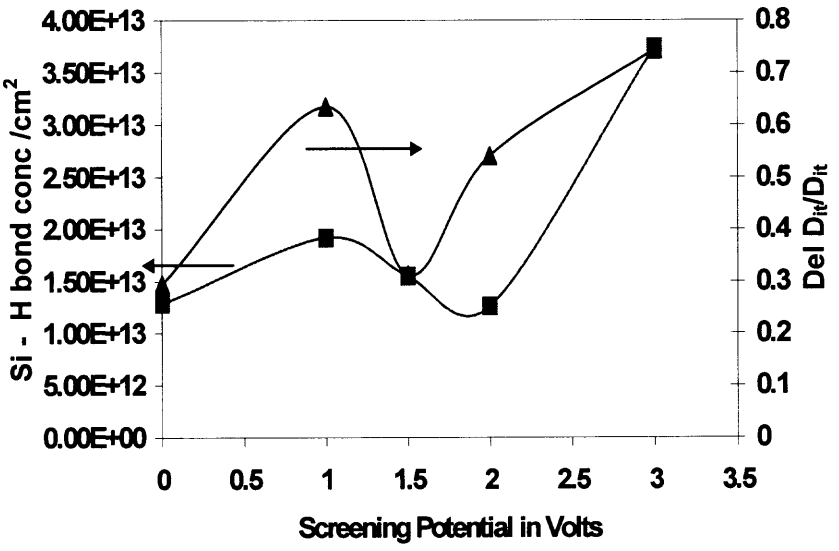


Figure 5.3 Concentration of Si-H bonds for gate injection after DC stress for antenna ratio 50050.

5.3.2 Substrate injection

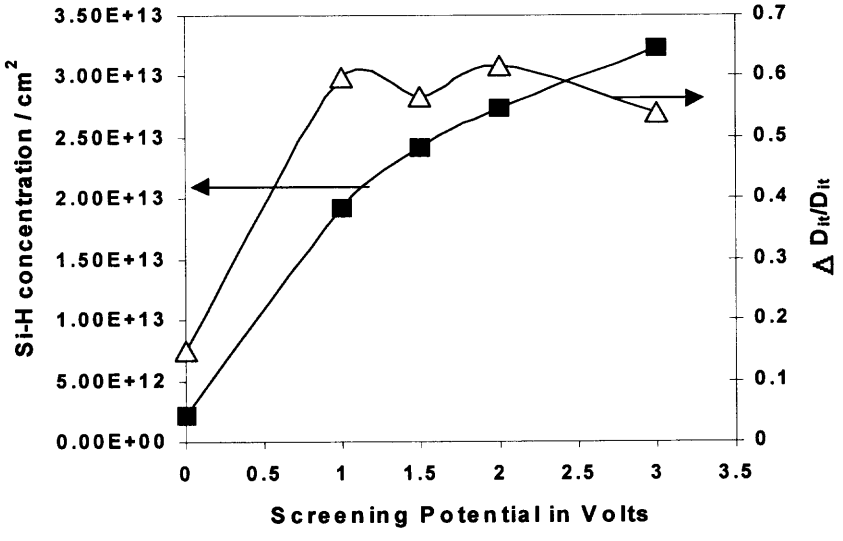


Figure 5.4 Concentration of Si-H bonds for substrate injection after DC stress.

Figure 5.4 shows the concentration of Si-H bonds along with $\Delta D_{it}/D_{it}$ as a function of screening potential immediately after the DC stress for substrate injection. As per $\Delta D_{it}/D_{it}$, effective screening potential is found to be in the order of 1 to 1.5 V for substrate injection. The Si-H bond concentration does not follow D_{it} during screening. The electron-hole pairs are generated at the gate-SiO_2 interface (anode) and hence there is no direct impact on the Si-H bond concentration at the Si-SiO_2 interface. At screening, therefore, the dominant mechanism that contributes to D_{it} is the creation of electrically active sites rather than Si-H bond breaking. At higher screening potentials, creation of electrically active sites close to interface and in bulk SiO_2 becomes dominant. These sites contribute significantly to D_{it} rather than breaking the Si-H bonds. Similar trends were noticed for other groups of transistors with antenna ratios, 10060 and 50050. Figure 5.5 and Figure 5.6 plot the concentration of Si-H bonds with $\Delta D_{it}/D_{it}$ as a function of screening potential for the antenna ratios 10060 and 50050 respectively.

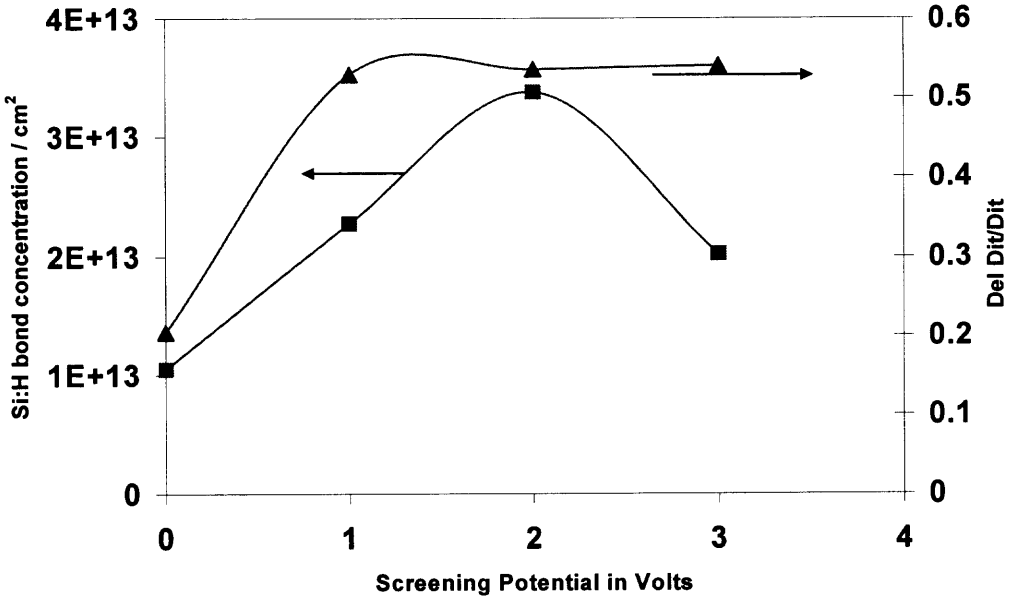


Figure 5.5 Concentration of Si-H bonds for substrate injection after DC stress for antenna ratio 10060.

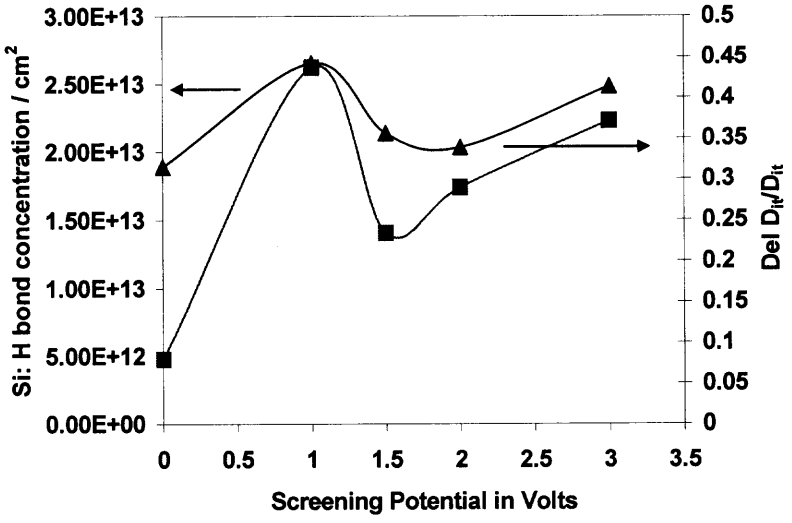


Figure 5.6 Concentration of Si-H bonds for substrate injection after DC stress for antenna ratio 50050.

5.4. Si-H Bond Concentration After Hot Electron Stress

5.4.1 Effect of Si-H Bond Concentration with Stress Time

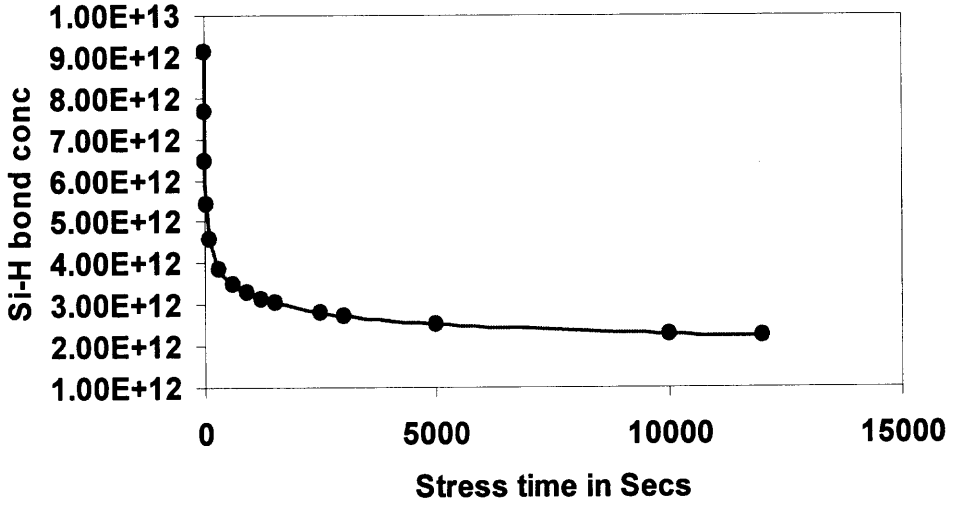


Figure 5.7 Effect of hot electron stress time on Si-H bonds.

Figure 5.7 shows the effect of hot electron stress time on the concentration of Si-H bonds. It is seen that the concentration of the bonds at the interface decrease as the stress time is increased, indicating the effect on Si-H bonds to be an exponential function of time.

5.4.2 Effect of Si-H Bond Concentration on Gate Injection

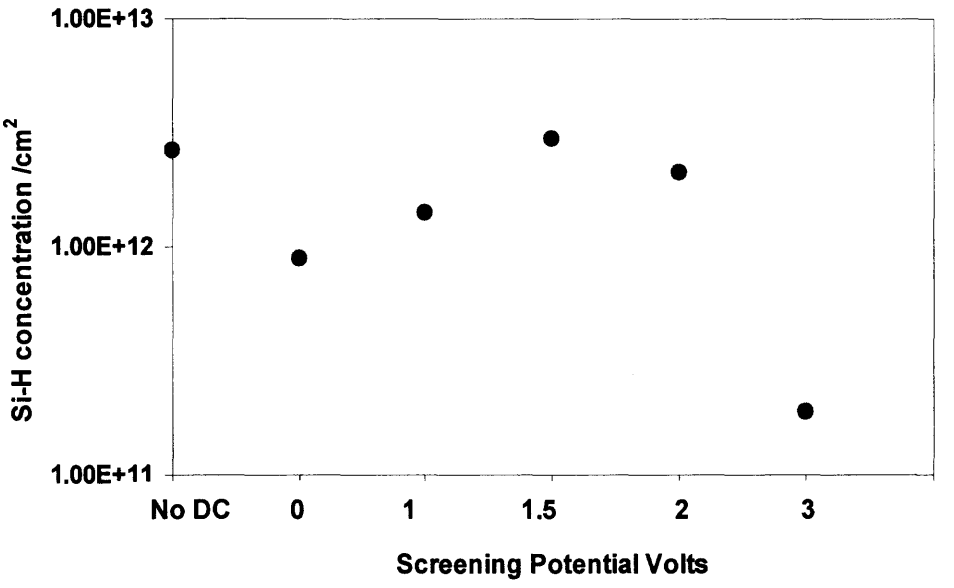


Figure 5.8 Concentration of Si-H bonds after hot electron stress time of antenna ratio 2009.

To confirm the screening of Si-H bonds during gate injection, devices were subjected to hot carrier stress during which two dominant mechanisms play key roles at the interface - the donor or the acceptor sites are being neutralized in the oxide affecting the interface trap generation and release of interfacial hydrogen that contributes to interface traps. Figure 5.8 shows the change in concentration of the Si-H bonds on the transistors earlier subjected to DC stress under applied screening potentials in gate injection mode. It is seen that under effective screening, the interface near drain junctions are protected which helps to reduce the Si-H bond-breaking phenomenon.

5.5 Impact on Source and Drain of the Transistor

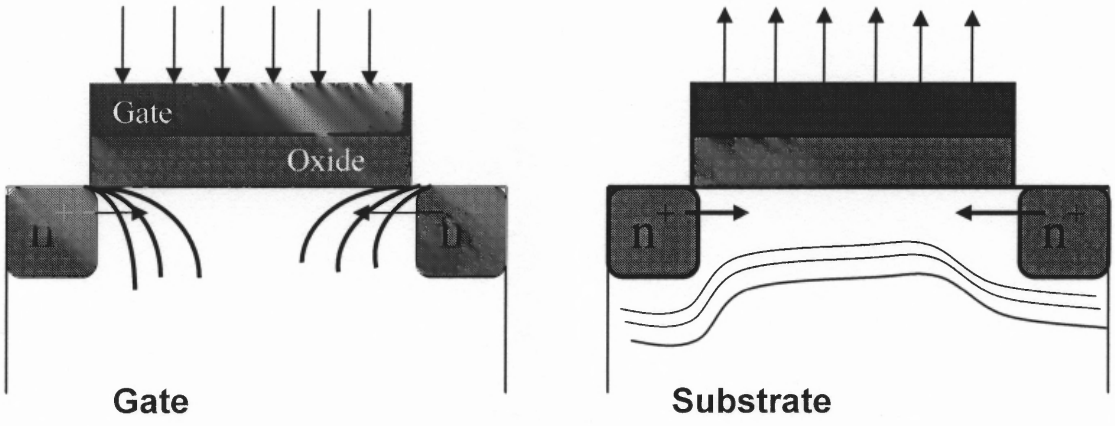


Figure 5.9 Impact on the depletion layer widths of the transistor due to the impact of high field and screening potential.

The protection of drain and source edges are possible due to the extended depletion layer near the Si-SiO_2 interface when the screening potential is applied during gate injection. For example, if L_0 is the as drawn length of a transistor, then with depletion regions formed due to reverse biased voltages at source and drain L_0 is reduced by $(W_S + W_D)$ where W_S and W_D are the drain and source depletion lengths. W_S or W_D is given by $[\{2\varepsilon_0\varepsilon_{Si}(V_{bi} + \psi_S + V_{D,S} - 2kT/q)\}/qN_A]^{1/2}$ where ε_0 is the free space permittivity, ε_{Si} is the silicon dielectric constant, V_{bi} is the built-in potential between the source/drain and substrate junction, ψ_S is the surface potential, $V_{D,S}$ is the screening potential, k is Boltzmann's constant, T is the temperature, q is electronic charge and N_A is the substrate doping. The effective channel length L_{eff} is then given by $L_{eff} = L_0 - (W_S + W_D)$. Because of the variation of surface potential during gate injection, the extended depletion layer for lower screening potentials was unable to screen the drain edge. The extended depletion region to the interface under the effective screening potentials (1.5-2 V), therefore, influences the concentration of the Si-H bonds.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

Potential problems occurring from the antenna connected to source and drain during the plasma processing has been discussed. The floating potentials developed at the source and drain can screen the hot carrier lifetime in plasma-processed devices. The screening effect depends on various parameters, namely, the size of the antenna ratios, the polarity of the stress involved and the oxide quality. This effect has been found to have a significant impact on the hot carrier lifetime of the transistor, indicating as an important factor that needs to be considered during VLSI (plasma) processing. The screening of Si-H bonds during high field injection suggest that Si-H bond breaking mechanism during interface state generation is dependent on the polarity of the current stress and the screening potential applied. Hot carrier stress further confirmed the results.

Since the hot carrier reliability could limit the performance of devices with alternate high-k-dielectric materials, this work can elucidate further some of the reliability issues in devices with high-k dielectrics. This scope of research can also be extended to the study of Si-D bonds at Si-SiO_2 interface, in deuterium annealed/implanted devices.

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